CONVERTING THREE-STAGE PSEUDO-CLASS AB AMPLIFIERS TO
TRUE CLASS AB AMPLIFIERS

BY
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“CONVERTING THREE-STAGE PSEUDO-CLASS AB AMPLIFIERS TO TRUE CLASS AB AMPLIFIERS,” a dissertation prepared by PUNITH REDDY SURKANTI in partial fulfillment of the requirements for the degree, Master of Sciences has been approved and accepted by the following:

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DEDICATION

Dedicated to my mother Lalitha, father Madhava Reddy, sister Dr. Avanthi Reddy, my advisor Dr. Paul Furth and all my friends and family members.
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I would like to thank my parents Lalitha Surkanti and Madhava Reddy Surkanti for their support and their confidence. And my sister Dr. Avanthi Reddy Surkanti, who encouraged me to complete my Master’s in USA. She is a role model for me, who inspired me for what I have done.

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ABSTRACT

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BY

PUNITH REDDY SURKANTI, B.Tech

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Specialization in Electrical Engineering
New Mexico State University
Las Cruces, New Mexico, 2011
Dr. Paul M. Furth, Chair

A widely-adopted low voltage, low transistor count, high gain and wide swing three-stage pseudo-class AB amplifier is converted to a true class AB amplifier. The conversion is made possible by using gate-drain feedback to combine two inverting common-source amplifiers to form a single non-inverting amplifier. The circuit is stable for a wide range of capacitive and resistive loads. The class AB amplifier has a dc gain of 81.7dB and unity gain frequency of 6.58MHz when driving a load of 100pF||10kΩ. Maximum output currents are 1.12mA of sourcing and 1.14mA sinking current from the positive and negative power rail respectively with a quiescent current of 95µA, when operating from ±1.25V power supply and driving a 1kΩ load. This demonstrates the class AB characteristic of the amplifier.
Both pseudo-class AB and true class AB amplifiers were fabricated in a 0.5\(\mu\)m CMOS 2P3M technology and measured to characterize their differences.

A novel inverting current buffer compensation technique for multi-stage amplifiers is proposed. The compensation capacitor from the output is connected to the bias node that helps in increasing the bandwidth and improving the power supply rejection ratio. This also helps in increasing the driving capability for a wide range of load capacitor values.
TABLE OF CONTENTS

LIST OF TABLES xii

LIST OF FIGURES xiii

1 INTRODUCTION 1

2 LITERATURE REVIEW 4
   2.1 Multi-Stage Amplifiers 4
   2.2 Compensation Techniques 5
      2.2.1 Miller Compensation 5
      2.2.2 Ahuja Compensation 7
      2.2.3 Nested Miller Compensation 8
      2.2.4 Reverse-Nested Miller Compensation 9
      2.2.5 Miller Compensation with Inverted Current-Buffer 10
   2.3 Class AB Amplifiers 11
      2.3.1 I-I-N Pseudo Class-AB Amplifier [1] 11
      2.3.2 Pseudo-Class AB to True Class AB Amplifier using Adaptive Biasing proposed in [2] 13

3 DESIGN AND SIMULATIONS 15
   3.1 I-I-N Three-stage Pseudo-Class AB Amplifier 15
      3.1.1 Operation 15
# LIST OF TABLES

<table>
<thead>
<tr>
<th>Table</th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.1</td>
<td>Dimensions of transistors</td>
<td>17</td>
</tr>
<tr>
<td>3.2</td>
<td>Equations of Poles and Zeros of I-I-N Pseudo-Class AB Amplifier</td>
<td>19</td>
</tr>
<tr>
<td>3.3</td>
<td>Dimensions of transistors</td>
<td>22</td>
</tr>
<tr>
<td>3.4</td>
<td>Equations of Poles and Zeros of I-N-I Pseudo-Class AB Amplifier</td>
<td>24</td>
</tr>
<tr>
<td>3.5</td>
<td>Dimensions of transistors</td>
<td>26</td>
</tr>
<tr>
<td>3.6</td>
<td>Equations of Poles and Zeros of Amplifier with Inverted Current Buffer Compensation</td>
<td>29</td>
</tr>
<tr>
<td>3.7</td>
<td>Simulated Results</td>
<td>36</td>
</tr>
<tr>
<td>3.8</td>
<td>Dimensions of transistors of I-N-I Class AB Amplifier</td>
<td>38</td>
</tr>
<tr>
<td>3.9</td>
<td>Equations of Poles and Zeros of I-N-I Class AB Amplifier</td>
<td>42</td>
</tr>
<tr>
<td>3.10</td>
<td>Dimensions of transistors Proposed Class AB Amplifier</td>
<td>44</td>
</tr>
<tr>
<td>3.11</td>
<td>Equations of Poles and Zeros of Proposed Class AB Amplifier</td>
<td>48</td>
</tr>
<tr>
<td>3.12</td>
<td>Simulated Results</td>
<td>56</td>
</tr>
<tr>
<td>4.1</td>
<td>Measured Results</td>
<td>65</td>
</tr>
<tr>
<td>I</td>
<td>Pin Description of the Fabricated Chip</td>
<td>72</td>
</tr>
</tbody>
</table>
## LIST OF FIGURES

<table>
<thead>
<tr>
<th>Figure</th>
<th>Title</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.1</td>
<td>Miller effect on resistance across the inverting amplifier.</td>
<td>3</td>
</tr>
<tr>
<td>2.1</td>
<td>Miller compensation.</td>
<td>6</td>
</tr>
<tr>
<td>2.2</td>
<td>Miller compensation with nulling resistor.</td>
<td>7</td>
</tr>
<tr>
<td>2.3</td>
<td>Ahuja current-buffer compensation.</td>
<td>8</td>
</tr>
<tr>
<td>2.4</td>
<td>Nested Miller compensation.</td>
<td>9</td>
</tr>
<tr>
<td>2.5</td>
<td>Reverse-nested Miller compensation.</td>
<td>9</td>
</tr>
<tr>
<td>2.6</td>
<td>Inverted current-buffer compensation.</td>
<td>10</td>
</tr>
<tr>
<td>2.7</td>
<td>Pseudo-class AB amplifier from [1].</td>
<td>12</td>
</tr>
<tr>
<td>2.8</td>
<td>Class AB amplifier with adaptive biasing.</td>
<td>13</td>
</tr>
<tr>
<td>3.1</td>
<td>Schematic of I-I-N three-stage pseudo-class AB amplifier.</td>
<td>16</td>
</tr>
<tr>
<td>3.2</td>
<td>Architecture of three-stage pseudo-class AB amplifier in Fig. 3.1.</td>
<td>18</td>
</tr>
<tr>
<td>3.3</td>
<td>Small-signal model of three-stage pseudo-class AB amplifier in Fig. 3.1</td>
<td>19</td>
</tr>
<tr>
<td>3.4</td>
<td>Schematic of I-N-I three-stage pseudo-class AB amplifier.</td>
<td>20</td>
</tr>
<tr>
<td>3.5</td>
<td>Architecture of three-stage pseudo-class AB amplifier in Fig. 3.4.</td>
<td>22</td>
</tr>
<tr>
<td>3.6</td>
<td>Small-signal model of three-stage pseudo-class AB amplifier in Fig. 3.4</td>
<td>23</td>
</tr>
<tr>
<td>3.7</td>
<td>Schematic of three-stage pseudo-class AB amplifier with inverted current buffer compensation.</td>
<td>26</td>
</tr>
<tr>
<td>3.8</td>
<td>Architecture of three-stage pseudo-class AB amplifier with inverted current buffer compensation.</td>
<td>27</td>
</tr>
<tr>
<td>Section</td>
<td>Title</td>
<td>Page</td>
</tr>
<tr>
<td>---------</td>
<td>------------------------------------------------------------------------</td>
<td>------</td>
</tr>
<tr>
<td>3.9</td>
<td>Small-signal model of three-stage pseudo-class AB amplifier with inverted current buffer compensation.</td>
<td>28</td>
</tr>
<tr>
<td>3.10</td>
<td>AC analysis test bench of three-stage pseudo-class AB amplifiers without and with inverting current-buffer compensation.</td>
<td>30</td>
</tr>
<tr>
<td>3.11</td>
<td>Frequency plot of I-I-N three-stage pseudo-class AB amplifier.</td>
<td>30</td>
</tr>
<tr>
<td>3.12</td>
<td>Frequency plot of I-N-I three-stage pseudo-class AB amplifier.</td>
<td>31</td>
</tr>
<tr>
<td>3.13</td>
<td>Frequency plot of I-I-N three-stage pseudo-class AB amplifier with inverted current-buffer compensation.</td>
<td>31</td>
</tr>
<tr>
<td>3.14</td>
<td>Transient analysis test bench in non-inverting configuration.</td>
<td>32</td>
</tr>
<tr>
<td>3.15</td>
<td>Transient output of I-I-N three-stage pseudo-class AB amplifier.</td>
<td>33</td>
</tr>
<tr>
<td>3.16</td>
<td>Transient output of I-N-I three-stage pseudo-class AB amplifier.</td>
<td>33</td>
</tr>
<tr>
<td>3.17</td>
<td>Transient output of I-I-N three-stage pseudo-class AB amplifier with inverting current-buffer compensation.</td>
<td>34</td>
</tr>
<tr>
<td>3.18</td>
<td>Test bench for finding PSRR.</td>
<td>35</td>
</tr>
<tr>
<td>3.19</td>
<td>Frequency plot of PSRR with and without inverted current-buffer compensation.</td>
<td>35</td>
</tr>
<tr>
<td>3.20</td>
<td>Schematic of three-stage class AB amplifier.</td>
<td>38</td>
</tr>
<tr>
<td>3.21</td>
<td>Architecture of three-stage class AB amplifier.</td>
<td>40</td>
</tr>
<tr>
<td>3.22</td>
<td>Small-signal model of three-stage class AB amplifier.</td>
<td>41</td>
</tr>
<tr>
<td>3.23</td>
<td>Schematic of proposed three-stage class AB amplifier.</td>
<td>43</td>
</tr>
<tr>
<td>3.24</td>
<td>Architecture of the proposed three-stage class AB amplifier.</td>
<td>45</td>
</tr>
<tr>
<td>3.25</td>
<td>Small-signal model of the proposed three-stage class AB amplifier.</td>
<td>47</td>
</tr>
<tr>
<td>3.26</td>
<td>DC analysis test bench of proposed three-stage class AB amplifier.</td>
<td>49</td>
</tr>
<tr>
<td>3.27</td>
<td>DC currents of I-I-N three-stage pseudo-class AB amplifier.</td>
<td>50</td>
</tr>
<tr>
<td>3.28</td>
<td>DC currents of I-N-I three-stage pseudo-class AB amplifier.</td>
<td>50</td>
</tr>
<tr>
<td>3.29</td>
<td>DC currents of I-N-I three-stage class AB amplifier.</td>
<td>51</td>
</tr>
<tr>
<td>3.30</td>
<td>DC currents of proposed three-stage class AB amplifier.</td>
<td>51</td>
</tr>
</tbody>
</table>
3.31 AC analysis test bench of proposed three-stage class AB amplifier.

3.32 Frequency plot of I-I-N three-stage class AB amplifier.

3.33 Frequency plot of I-N-I proposed class AB amplifier.

3.34 Transient analysis test bench in non-inverting configuration of proposed three-stage class AB amplifier.

3.35 Transient output of I-N-I three-stage class AB amplifier.

3.36 Transient output of proposed class AB amplifier.

4.1 Layout of I-I-N pseudo-class AB amplifier.

4.2 Layout of I-I-N pseudo-class AB amplifier with inverted current-buffer compensation.

4.3 Layout of I-N-I pseudo-class AB amplifier.

4.4 Layout of proposed class AB amplifier.

4.5 Layout of overall chip.

4.6 Hardware transient output of I-I-N pseudo-class AB amplifier.

4.7 Hardware transient output of I-I-N pseudo-class AB amplifier with inverted current-buffer compensation.

4.8 Hardware transient output of I-N-I pseudo-class AB amplifier.

4.9 Hardware transient output of proposed class AB amplifier.

A.1 Test bench for measuring transient response of the amplifier.

A.2 Test bench for measuring PSRR of the amplifier.

A.3 Test bench for measuring DC Currents of the amplifiers.
Chapter 1

INTRODUCTION

Class AB amplifiers have a wide range of applications in portable electronic devices. They are used in the design of circuits such as audio amplifiers, motor drivers and LED & LCD drivers [3]. Most of these applications require class AB amplifiers with low power, high efficiency, and stability for a wide range of loads.

A widely-adopted low voltage, low transistor-count, high-gain and wide-swing three-stage pseudo-class AB amplifier is proposed in [1]. We designed a NMOS version of that pseudo-class AB amplifier and analysed the circuit using the location of poles and zeros. We introduced a novel inverted current-buffer compensation to that pseudo class AB amplifier to increase stability with low compensation capacitor values. Inverted current-buffer helps in inserting a LHP zero and improves phase margin. The inverted current-buffer compensation also helps in increasing Power-Supply Rejection Ratio (PSRR).

The pseudo-class AB amplifier has inverting, inverting and non-inverting gain cascaded stages. The pseudo-class AB amplifier has a NMOS current mirror in the output-stage and, therefore, the quiescent current increases with the output sourcing current. We re-designed the circuit with same number of transistors and removed the current mirror in the output stage. The modified amplifier has inverting, non-inverting and inverting gain cascaded stages. The drawback of this amplifier is the quiescent current increase with the increase in output sourcing cur-
rent. This is because of the huge current through the second-stage common-source amplifier.

We limited the current in the second stage to the bias current by adding the cascaded transistors to the current mirror. The new design has nearly constant quiescent current irrespective of changes in the output current. Therefore, this amplifier is designated as a true class AB amplifier. The class AB amplifier is stable with nested inverting current-buffer compensation for wide range of load capacitance. But the drawback of this class AB amplifier is that the quiescent for sourcing current is slightly higher than the quiescent current for sinking current. This is because of the cascoded current mirror in the second-stage.

Finally, we proposed a true class AB amplifier which has inverting, non-inverting and inverting gain cascade stages. The non-inverting common-source stage is designed by using gate-drain feedback to combine two inverting common-source amplifiers. Gate-drain feedback resistor across the inverting common-source amplifier helps in cancelling its effect for the overall second-stage. Miller effect splits the impedance across the amplifier to input node and output node as shown in Fig. 1.1. Therefore, the resistor to the input side decreases by the gain of the amplifier. If this amplifier is cascaded to an amplifier, then the gain of first stage is cancelled. This is because of the decrement of the resistor value by gain of the next amplifier; therefore, the overall gain is positive.

The proposed class AB amplifier is compensated with both nested and reverse-nested Miller compensation to increase the stability. The inverted current-buffer compensation has no effect for this amplifier because of forming both negative and positive feedback network with the proposed compensation capacitor.

Since current through all the internal stages are limited to the bias current, the total quiescent current is nearly constant irrespective of the output current.
Unlike the class AB amplifier discussed earlier, the proposed class AB amplifier has the same quiescent current for both sourcing and sinking current.

The proposed class AB is stable for a wide range of capacitive and resistive loads. The bandwidth of the proposed class AB amplifier is increased by 60% when compared to the I-I-N pseudo-class AB amplifier and 25% compared to the pseudo-class AB amplifier with inverting current buffer compensation. Maximum output currents are 1.12mA of sourcing and 1.14mA sinking current from the positive and negative power rail respectively for all the amplifiers when operating from ±1.25V power supply and driving a 1kΩ load. The maximum quiescent current of I-I-N and I-N-I pseudo-class AB amplifier is nearly 300µA and 483µA, respectively. The maximum quiescent current of proposed class AB amplifier is nearly 95µA. This demonstrates the true class AB characteristic of the proposed amplifier. All the amplifiers are fabricated in a 0.5µm CMOS 2P3M technology and measured to characterize their differences.
Chapter 2

LITERATURE REVIEW

This section discusses the work done in the literature. The different types of compensation techniques used for multi-stage amplifiers, class AB amplifiers, pseudo-class AB amplifiers and a topology in literature to convert pseudo-class AB amplifier to a true class AB amplifier.

2.1 Multi-Stage Amplifiers

As technology advances, parameters such as size of the transistor and supply voltage are decreasing. This results in the reduction in gain for a single-stage amplifier. The best method to achieve high gain is by cascading amplifiers, where the total gain is the product of gains of each stage. The output-swing is maximized for common-source output stages, resulting in rail-to-rail output swing \[4\]. However, as the number of stages increases, the stability of the overall amplifier becomes more difficult to guarantee for a wide range of capacitive loads.

An amplifier is said to be stable, if the gain crosses unity before the phase drops to -180°. The maximum available phase at unity-gain frequency \(f_t\) is known as the phase margin. Phase margin helps in determining stability; 60° of phase margin typically implies a stable system with fast time-domain response and little to one ringing. 45° of phase margin implies some ringing in the time-domain response. Less than 45° is considered undesirable, as ringing increases and normal variations in process parameters could result in an unstable system.
The number and position of poles and zeros effects the phase margin. The number of poles increases with the number of cascaded stages. Left-Half-Plane (LHP) poles decrease the gain with a slope of -20dB/decade and drops the phase by 90°. If a system has two low frequency poles, then the phase drops towards -180° before the gain cross $f_t$. This makes the system unstable. LHP zeros are inserted to improve the stability. A LHP zero increases the gain by 20dB/decade and increases the phase by 90°. If a system with two poles has a LHP zero, then the effect of one of the poles is cancelled by proper placement of the zero. If cancellation is not possible, then the zero often helps in improving the phase margin.

Compensation techniques are used to split the poles and to insert the zeros. Careful compensation helps in guaranteeing stability of the overall amplifier for a wide range of capacitive loads. The complexity of the compensation network increases with the number of cascaded stages [5]. Different compensation techniques are used to improve the stability and some of them are discussed in the next section.

2.2 Compensation Techniques

Amplifiers are compensated in different manners, depending on the number of stages. Miller compensation and Ahuja compensation are used in amplifiers with two or more cascaded stages, whereas, nested Miller compensation and reverse-nested Miller compensation are used in amplifiers with three or more cascaded stages.

2.2.1 Miller Compensation

Miller compensation is widely used and discussed in literature [6, 4, 7, 8]. Miller compensation is used in a two-stage amplifier as shown in Fig. 2.1. A capacitor $C_C$ is connected between output node and the internal node $V_1$. This splits
the two poles; the dominant one to lower frequencies and the non-dominant one to higher frequencies. The existence of a feed-forward path from $V_1$ to $V_{OUT}$ creates a Right-Half-Plane (RHP) zero. A RHP zero increases the gain by 20dB/decade and drops the phase by $90^\circ$. RHP zeros are more dangerous than LHP poles, as they tend to decrease the phase margin. The equation of two LHP poles is

$$\omega_{P1} = \frac{1}{AV_2 \cdot R_1 \cdot CC}. \quad (2.1)$$

$$\omega_{P2} = \frac{AV_2}{(R_1 + RC) \cdot C_{OUT}}. \quad (2.2)$$
To remove the RHP zero, Miller capacitor with a nulling resistor in series is used as shown in Fig. 3.1. The equation of the zero is

$$\omega_{Z1} = \frac{1}{C_C \cdot \left( \frac{1}{g_{M2}} - R_C \right)}.$$  \hfill (2.3)

If the value of the resistor $R_C$ is equal to $\frac{1}{g_{M2}}$, where $g_{M2}$ is transconductance of second stage, then the zero moves to infinity. If $R_C$ increases, then the RHP zero moves to the LHP, which can be used to improve the phase margin and increase stability.

### 2.2.2 Ahuja Compensation

A Miller capacitor with a current-buffer in series helps in increasing the stability, phase margin and bandwidth of the amplifier. Instead of an extra current-buffer circuit, the cascoded transistor is used as the current-buffer as shown in Fig. 2.3. The cascoded transistor is a common-gate amplifier which has a positive
gain of \( g_M R_1 \) and the input impedance is \( \frac{1}{g_M} \) as proposed in [9]. Therefore the overall feedback is negative feedback. This creates a LHP zero given by

\[
\omega_{Z1} = \frac{g_{M2}}{C_C}.
\]  

(2.4)

where \( g_{M2} \) is the transconductance of second-stage.

2.2.3 Nested Miller Compensation

Miller compensation is used in two-stage amplifiers. More than one Miller compensation network can be used for three-stage amplifiers. Suppose, a three-stage amplifier has an inverted amplifier at first-stage, non-inverting amplifier at the second-stage and an inverting amplifier at the third-stage as shown in Fig. 2.4. Miller compensation capacitor \( C_{C1} \) from node \( V_{OUT} \) to the first-stage output node \( V_1 \) and \( C_{C2} \) from node \( V_{OUT} \) to the second-stage output node \( V_2 \) with a single resistor \( R_C \) are connected as shown in Fig. 2.4. Since the second and third stages
have non-inverting and inverting gains, respectively; compensation $C_{C1}$ and $C_{C2}$ form negative feedback. The compensation appears to be Miller compensation inside Miller compensation; therefore, the compensation is known as nested Miller compensation [10, 11, 12]. This compensation creates two LHP zeros and proper placement of them cancels the effect of two non-dominant poles.

2.2.4 Reverse-Nested Miller Compensation

Figure 2.5: Reverse-nested Miller compensation.
Suppose a three-stage amplifier has inverting gain amplifier at first-stage, inverting amplifier at second-stage and non-inverting amplifier at the third-stage as shown in Fig. 2.5. Miller compensation capacitor $C_{C1}$ from node $V_1$ to output node $V_{OUT}$ and $C_{C2}$ from node $V_1$ to second stage output node $V_2$ with a single resistor $R_C$ are connected as shown in Fig. 2.5. Since the second and third stages has inverting and non-inverting gains respectively, the compensation $C_{C1}$ and $C_{C2}$ form negative feedback. The compensation appears to be a Miller compensation inside the Miller compensation in reverse direction; therefore, the compensation is known as reverse-nested Miller compensation [13, 14, 15, 1]. The compensation creates two LHP zeros and proper placement of them cancels the effect of two non-dominant poles.

![Figure 2.6: Inverted current-buffer compensation.](image)

### 2.2.5 Miller Compensation with Inverted Current-Buffer

Multi-stage amplifiers can be compensated by different compensation techniques. Similar to the Ahuja compensation proposed in [9] the current-buffer is replaced with inverted current-buffer. The output transistor $M_{N_{1,4}}$ of the current mirror in the differential amplifier is used as an inverted current-buffer. The compensation capacitor is connected from node $V_3$ to the gate of current mirror as
shown in Fig. 2.6. The input impedance of the inverted current-buffer is $\frac{1}{G_m}$ and this helps in creating LHP zeros. This also helps in improving the bandwidth and wide driving capability.

### 2.3 Class AB Amplifiers

Class AB amplifiers have a wide range of applications in portable electronic devices. They are used in the design of circuits such as audio amplifiers, motor drivers and LED & LCD drivers [3]. Most of these applications require class AB amplifiers with low power, high efficiency, and stability for a wide range of loads. They are also required to have rail-to-rail operation when driving low resistive loads. Class AB amplifiers can generate large output currents that are much greater than the quiescent current of the output stage, thereby maintaining low static power consumption [16]. As the power supply is decreasing the operating speed and the dynamic range of analog amplifier is becoming more limited [17]. High slew rate is also an important factor for a class AB amplifiers used as LCD drivers [18]. Achieving all of these performance requirements simultaneously is becoming more complex for designers.

The class AB amplifier can deliver huge output current with very low quiescent. The output current is not limited by the bias current and therefore has very high efficiency. The pseudo-class AB amplifier can also deliver huge output currents that are not limited by the bias current, but the quiescent current is huge. The quiescent current is proportional to the output current and therefore has a low current efficiency. A three-stage pseudo-class AB amplifier is described in the next section.

#### 2.3.1 I-I-N Pseudo Class-AB Amplifier [1]

The pseudo-class AB amplifier shown in the Fig. 2.7 is three-stage amplifier proposed in [1]. First-stage of the amplifier is a folded cascode amplifier, that
has a huge gain and wide-swing. The next two stages are inverting and non-inverting common-source stages respectively. A feed-forward path is formed by NMOS inverting common-source amplifier $M_{N4}$ from $V_1$ node to output node. This provides the push-pull action to the pseudo-class AB amplifier. The amplifier has huge sourcing and sinking currents. The quiescent current increase with the increase in sourcing current, because of the presence of PMOS current mirror in the output stage. Therefore the efficiency of the amplifier is too low. As the number of stages are three, the complexity of compensation increases. Miller compensation, Ahuja compensation and inverted current buffer compensations are used to stabilize the pseudo-class AB amplifier shown in Fig. 2.7.

In order to decrease the quiescent current in Fig. 2.7 adaptive biasing technique is used. This to converts the pseudo-class AB amplifier to a true class AB amplifier and is discussed in following section.
2.3.2 Pseudo-Class AB to True Class AB Amplifier using Adaptive Biasing proposed in [2]

The three stage amplifier proposed in [1] has high quiescent current with the sourcing current. Pseudo-class AB amplifier is converted to a true class AB amplifier using adaptive biasing technique is proposed in [19, 2]. The schematic of the true class-AB amplifier is shown in Fig. 2.8. The PMOS current mirror in the last stage is modified with the Widlar current mirror. A resistor is connected to the source of the input transistor $M_{P3}$ of the current mirror. If the current through the output transistor $M_{P4}$ is huge then $V_{SG}$ is too high. The presence of resistor $R_{ad1}$ at the source, the $V_{SG}$ of $M_{P3}$ is goes low. Therefore the current through the transistor $M_{P3}$ is very low. Similarly, for low currents through $M_{P4}$, the transistor $M_{P3}$ operated in cut-off and the resistor $R_{ad2}$ provides current to $M_{N3}$ transistor.

The adaptive biasing overcomes the drawback of the pseudo-class AB amplifier, by decreasing the quiescent current for huge sourcing current. Therefore the amplifier shown in Fig. 2.8 is characterized as a true class AB amplifier.
In this project, we analysed two widely-used pseudo-class AB amplifiers that have high-gain multi-stage amplifier with a simple biasing circuit, low transistor-count and wide output-swing. The amplifier can operate with low supply voltages and currents. Therefore, the amplifier is widely reported in [20, 21, 13, 22, 19, 2]. We improved the topology of the pseudo-class AB amplifiers and converted to a true class AB amplifiers.
Chapter 3

DESIGN AND SIMULATIONS

Two different pseudo-class AB amplifiers are discussed in this section that are converted to true class AB amplifiers. Both of these pseudo-class AB amplifiers are three-stage. One amplifier has inverting, inverting and non-inverting (I-I-N) cascade stages. The other amplifier has inverting, non-inverting and inverting (I-N-I) cascade stages. Both the amplifiers are widely used because of high-gain, low transistor-count, simple biasing circuit and wide output-swing. The amplifiers can operate with low supply voltage, bias current and can generate huge output currents.

3.1 I-I-N Three-stage Pseudo-Class AB Amplifier

A three-stage pseudo-class AB amplifier shown in Fig. 3.1 is the NMOS version of the circuit in [1]. The first stage is a differential amplifier and the next two stages are common-source amplifiers. The first common-source amplifier has negative gain and the second one has positive gain. The PMOS transistor $M_{PF}$, which is an inverting common-source amplifier, creates a feed-forward path from the intermediate node to the final output to produce the push-pull action for the amplifier.

3.1.1 Operation

As the input $V_{IN+}$ increases, the current through the $M_{N1,2}$ increases results in the decrement of voltage at node $V_1$. Therefore the current through $M_{P2}$ and $M_{PF}$ increases. Since the transistor $M_{N2}$ can sink only bias current, the voltage
at node $V_2$ increases, resulting in decrease of gate voltage of the $M_{N3,1}$ transistor. This turns off the final stage NMOS transistor $M_{N3}$, since the gate of $M_{N3,1}$ is connected to $M_{N3}$. The PMOS transistor $M_{PF}$ forms a feed-forward path from the intermediate node $V_1$ to the output. Therefore, as $V_{IN+}$ increases, the amplifier delivers huge source current to the load.

Conversely, if $V_{IN-}$ increases then the voltage at node $V_1$ also increases, that turns off the PMOS transistor $M_{PF}$. Since the the voltage at node $V_1$ is increased, the voltage at node $V_2$ is decreased because of the presence of an inverting common-source amplifier. The gate voltage of $M_{N3,1}$ and $M_{N3}$ increases, results in the increase of sinking current through the output stage NMOS transistor $M_{N3}$.

This explains the push-pull action of the amplifier when $V_{IN+}$ and $V_{IN-}$ goes high respectively. The maximum sourcing current through $M_{PF}$ is limited by the common-mode input voltage applied to $V_{IN+}$ and $V_{IN-}$. On the other hand, the maximum sinking current through $M_{N3}$ is only limited by the supply voltage.
The last stage of the amplifier is a non-inverting common source amplifier. It comprises a NMOS current mirror formed by $M_{N3,1}$ and $M_{N3}$ with a dimension ratio of in 1:K. Since $M_{N3}$ is the output transistor it can pull a large sinking current, that results in correspondingly large current through the mirrored transistor $M_{N3,1}$. Thus the quiescent current is increases with the increase in output sinking current, resulting in the loss of current efficiency and power. Hence, the amplifier is designated as a pseudo-class AB amplifier.

<table>
<thead>
<tr>
<th>Table 3.1: Dimensions of transistors</th>
<th>I-I-N pseudo-class AB</th>
</tr>
</thead>
<tbody>
<tr>
<td>$M_{N1,1}, M_{N1,2}, M_{N2}, M_{N3,1}$</td>
<td>$10^{1\frac{1}{2}}, m = 2$</td>
</tr>
<tr>
<td>$M_{P1,1}, M_{P1,2}, M_{P2}$</td>
<td>$30^{1\frac{1}{2}}, m = 2$</td>
</tr>
<tr>
<td>$M_{N3}$ &amp; $M_{PF}$</td>
<td>$10^{1\frac{1}{2}}$ &amp; $30^{1\frac{1}{2}}, m = 8$</td>
</tr>
<tr>
<td>$M_{Nbias1}$</td>
<td>$10^{1\frac{1}{2}}, m = 4$</td>
</tr>
<tr>
<td>$M_{Nbias}$</td>
<td>$10^{1\frac{1}{2}}, m = 1$</td>
</tr>
<tr>
<td>$R_C$</td>
<td>$6.5k\Omega$</td>
</tr>
<tr>
<td>$C_{C1}, C_{C2}$</td>
<td>$7.5pF, 7.5pF$</td>
</tr>
</tbody>
</table>

Reverse-nested Miller compensation with resistor is used to stabilize the amplifier for a wide range of capacitive loads. The dimensions of all the transistors, resistors and capacitors are given in Table 3.1.

3.1.2 Small-Signal Analysis

The architecture and small-signal model of the circuit in Fig 3.1 is shown in Fig. 3.2 and Fig. 3.3 respectively. The transconductance of the first stage differential amplifier is denoted as $g_{M1}$ and the next stages are $g_{M2}$ and $g_{M3}$ respectively. The transconductance of feed-forward path is denoted as $g_{MF}$. The resistance
and capacitance at each stage’s output nodes are denoted as $R_1||C_1, R_2||C_2$ and $R_{OUT}||C_{OUT}$. The gain of the amplifier is approximately the product of the gains of all the three stages in cascade and is given by

$$Gain = g_{M1}R_1 \cdot (g_{M2}R_2 \cdot g_{M3}R_{OUT} + g_{MF}R_{OUT}). \quad (3.1)$$

The amplifier has four poles; the compensation capacitance $C_{C1}$ creates the dominant pole. The effect of the next two non-dominant poles can be nullified by proper placement of the two LHP zeros $\omega_{Z1}$ and $\omega_{Z2}$ created by the reverse-nested Miller compensation. The equation of all poles and zeros are shown in Table 3.2.
The two non-dominant pole locations discussed above are dependent on the output capacitor and the zeros are dependent on the compensation capacitor values. If the output capacitor is comparable to the compensation capacitor values, then the zeros can cancel the effect of poles. If the value of output capacitor is too large, then the poles move to low frequencies and the value of the compensation capacitor that cancel the poles may become prohibitively large. If cancelling is not possible, then phase margin and gain margin may decrease. Therefore the stability of the amplifier for wide range of capacitive loads with small values of compensation is limited. From simulation and experimental results, the amplifier
is stable for maximum load of 200pF with a total of 15pF compensation capacitance.

The last pole $\omega_{P4}$ is high frequency pole located far beyond the unity gain frequency and the effect of this pole on stability is assumed to be negligible.

To convert the pseudo-class AB amplifier shown in Fig. 3.1 to a class AB amplifier, the first step is to avoid current mirrors at the output stage. In order to avoid the current mirror at the output stage, a I-N-I three-stage pseudo class AB amplifier is designed and described in next section.

### 3.2 I-N-I Three-stage Pseudo-Class AB Amplifier

![Schematic of I-N-I three-stage pseudo-class AB amplifier](image)

Figure 3.4: Schematic of I-N-I three-stage pseudo-class AB amplifier.

The schematic of I-N-I three-stage pseudo-class AB amplifier shown in Fig. 3.4. The first stage is a differential amplifier and the next two stages are common-source amplifiers. The first common-source amplifier has positive gain and the second one has negative gain. The PMOS transistor $M_{PF}$, which is an inverting common-source amplifier, creates a feed-forward path from the intermediate node $V_1$ to the final output to produce the push-pull action for the amplifier. Nested Miller compensation with resistor is used to stabilize the amplifier for a
A wide range of capacitive loads. The dimensions of all the transistors, resistors and capacitors are given in Table 3.3.

### 3.2.1 Operation

As the input $V_{IN+}$ increases the current through the $M_{N1,2}$ increases results in the decrement of voltage at node $V_1$. Therefore the current through $M_{P2}$ and $M_{PF}$ increases. Since the node $V_1$ is connected to the second stage, which is a non-inverting common-source amplifier and the transistor $M_{P2,2}$ can source only bias current, the voltage at node $V_2$ also decreases. This turns off the final stage NMOS transistor $M_{N3}$. The PMOS transistor $M_{PF}$ forms a feed-forward path from the intermediate node $V_1$ to the output. Therefore the amplifier delivers huge source current if $V_{IN+}$ increases.

Conversely, if $V_{IN-}$ increases then the voltage at node $V_1$ also increases, turning off PMOS transistor $M_{PF}$. Since the the voltage at node $V_1$ is increased, the voltage at node $V_2$ increases because of the presence of a non-inverting common-source amplifier. This results in the increase of current through the output stage NMOS transistor $M_{N3}$. Therefore the amplifier has a huge sinking current if $V_{IN-}$ increases.

This explains the push-pull action of the amplifier when $V_{IN+}$ and $V_{IN-}$ increases respectively. The maximum sourcing current through $M_{PF}$ is limited by the common-mode input voltage applied to $V_{IN+}$ and $V_{IN-}$. On the other hand, the maximum sinking current through $M_{N3}$ is only limited by the supply voltage.

The second stage of the amplifier is a non-inverting common source amplifier. It comprises a NMOS current mirror formed by $M_{N2,1}$ and $M_{N2,2}$ with same dimensions. Since the first and second stages of the amplifier shown in Fig. 3.4 is biased with the bias current, the quiescent current seems to be nearly constant.
Figure 3.5: Architecture of three-stage pseudo-class AB amplifier in Fig. 3.4.

Table 3.3: Dimensions of transistors

<table>
<thead>
<tr>
<th></th>
<th>I-N-I pseudo-class AB</th>
</tr>
</thead>
<tbody>
<tr>
<td>$M_{N1,1}, M_{N1,2}, M_{N2,1}, M_{N2,2}$</td>
<td>$\frac{10}{1.2}, m = 2$</td>
</tr>
<tr>
<td>$M_{P1,1}, M_{P1,2}, M_{P2,1}, M_{P2,2}$</td>
<td>$\frac{30}{1.2}, m = 2$</td>
</tr>
<tr>
<td>$M_{Nbias1}$</td>
<td>$\frac{10}{1.2}, m = 4$</td>
</tr>
<tr>
<td>$M_{Nbias}, M_{Pbias}$</td>
<td>$\frac{10}{1.2}, \frac{30}{1.2}, m = 1$</td>
</tr>
<tr>
<td>$R_C$</td>
<td>$3k\Omega$</td>
</tr>
<tr>
<td>$C_{C1}, C_{C2}$</td>
<td>$7.25pF, 7.25pF$</td>
</tr>
</tbody>
</table>
irrespective of the output stage current. But the analysis shows that the amplifier is pseudo-class AB amplifier.

When the sourcing current increases then the voltage at node $V_1$ decreases. The current through the PMOS transistor $M_{P2,1}$ also increases. Since, the NMOS transistor $M_{N2,1}$ is not limited to bias current, the current through that branch is also increases. The increment in current also mirrors to $M_{N2,2}$ transistor because of the current mirror formed by $M_{N2,1}$ and $M_{N2,2}$. Since the current through PMOS transistor $M_{P2,2}$ is limited to bias current, the voltage at node $V_2$ decreases and turns off output NMOS transistor. Thus the quiescent current is increased when the output is sourcing, resulting in the loss of current efficiency and power; hence, the designation pseudo-class AB amplifier.

![Figure 3.6: Small-signal model of three-stage pseudo-class AB amplifier in Fig. 3.4](image)

### 3.2.2 Small-Signal Analysis

The architecture and small-signal model of the circuit in Fig. 3.4 is shown in Fig. 3.5 and Fig. 3.6 respectively. The transconductance of the first stage differential amplifier is denoted as $g_{M1}$ and the next stages are $g_{M2}$ and $g_{M3}$ respectively. The transconductance of feed-forward path is denoted as $g_{MF}$. The resistance and capacitance at each stage’s output nodes are denoted as $R_1||C_1$, $R_2||C_2$ and $R_{OUT}||C_{OUT}$. The gain of the amplifier is approximately the product of the gains
of all the three stages in cascade and is given by

\[ \text{Gain} = g_{M1}R_1 \cdot (g_{M2}R_2 \cdot g_{M3}R_{OUT} + g_{M3}R_{OUT}). \] \hspace{1cm} (3.2)

The amplifier has four poles; the compensation capacitance \( C_{C1} \) creates the dominant pole. The effect of the next two non-dominant poles \( \omega_{P2} \) and \( \omega_{P3} \) can be nullified by proper placement of the two LHP zeros \( \omega_{Z1} \) and \( \omega_{Z2} \) created by the reverse-nested Miller compensation. The equation of all poles and zeros are mentioned in Table 3.4.

<table>
<thead>
<tr>
<th>Poles</th>
<th>Zeros</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \omega_{P1} = \frac{1}{g_{M2}R_2 \cdot g_{M3}R_{OUT} \cdot R_1 \cdot C_{C1}} )</td>
<td>( \omega_{Z1} = \frac{1}{R_C \cdot (C_{C1} + C_{C2})} )</td>
</tr>
<tr>
<td>( \omega_{P2} = \frac{g_{M2} \cdot g_{M3}}{C_{C2} \cdot (g_{M3} + g_{MF} - g_{M2}(1 + \frac{R_C}{R_{OUT}}))} )</td>
<td>( \omega_{Z2} = \frac{g_{M2} \cdot g_{M3} \cdot (C_{C1} + C_{C2})}{(g_{MF} + g_{M3}) \cdot C_{C1} \cdot C_{C2}} )</td>
</tr>
<tr>
<td>( \omega_{P3} = \frac{C_{C2} \cdot (g_{M3} + g_{MF} - g_{M2}(1 + \frac{R_C}{R_{OUT}}))}{g_{M2} \cdot R_C \cdot C_{OUT}} )</td>
<td></td>
</tr>
<tr>
<td>( \omega_{P4} = \frac{1}{R_C \cdot C_{C1}} )</td>
<td></td>
</tr>
</tbody>
</table>

The two non-dominant pole locations discussed above are dependent on the output resistor and the zeros are dependent on the compensation capacitor values. If the \( R_{OUT} \) is less than \( R_C \), then the second and third LHP poles change to RHP poles creating oscillations in the amplifier. Therefore the value of the compensation resistor should be less than \( R_{OUT} \) and the amplifier is not stable for low values of output resistance. If the value of output resistor is close to value of compensation resistor \( R_C \), then the second pole moves to infinity. The third pole moves towards zero and the two LHP zeros helps in stabilizing the amplifier.
If the $R_{OUT}$ is much greater than the $R_C$, then the second and third pole are the two non-dominant poles that are cancelled by the proper placement of two zeros.

The last pole $\omega_p$ is high frequency pole located far beyond the unity gain frequency and the effect of this pole on stability is assumed to be negligible.

The stability and bandwidth of pseudo-class AB amplifiers are limited by the values of load capacitor or resistor. A novel compensation technique for multi-stage amplifiers is presented in the next section for improving stability, bandwidth and PSRR.

### 3.3 Inverted Current-Buffer Compensation

The inverted current buffer compensation technique is used in I-I-N pseudo-class AB amplifiers discussed earlier. The proposed compensation has a capacitor from the output node to the bias node and the bias transistor of second stage $M_{N2}$ acts as an inverted current buffer. The three stage amplifier shown in Fig. 3.1 is already compensated with reverse-nested Miller compensation. The proposed compensation technique is applied to the amplifier with a capacitor $C_{CB}$ from output node to the bias node $V_{BIAS}$ and is shown in Fig. 3.7.

The addition of proposed compensation reduces the capacitor values used in reverse nested Miller compensation to stabilize the amplifier. This results in increased bandwidth and PSRR. The dimensions of all the transistors, capacitors and resistors are mentioned in Table. 3.5.

#### 3.3.1 Inverted Current Buffer

The amplifier has three bias transistors, one is the diode connected transistor $M_{bias}$, that supplies bias currents to the rest of the circuit through $V_{Bias}$ node. The second one is the tail transistor $M_{Nbias1}$ of differential amplifier and the other one $M_{N2}$ that acts as a current source for the second stage common-source amplifier. The compensation capacitor $C_{CB}$ from output node is connected to $V_{Bias}$.
Figure 3.7: Schematic of three-stage pseudo-class AB amplifier with inverted current buffer compensation.

Table 3.5: Dimensions of transistors

<table>
<thead>
<tr>
<th>Transistor Configuration</th>
<th>I-I-N pseudo-class AB with $C_{CB}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$M_{N1,1}, M_{N1,2}, M_{N2}, M_{N3,1}$</td>
<td>$\frac{10}{1.2}, m = 2$</td>
</tr>
<tr>
<td>$M_{P1,1}, M_{P1,2}, M_{P2}$</td>
<td>$\frac{30}{1.2}, m = 2$</td>
</tr>
<tr>
<td>$M_{N3} &amp; M_{PF}$</td>
<td>$\frac{10}{1.2} &amp; \frac{30}{1.2}, m = 8$</td>
</tr>
<tr>
<td>$M_{Nbias1}$</td>
<td>$\frac{10}{1.2}, m = 4$</td>
</tr>
<tr>
<td>$M_{Nbias}$</td>
<td>$\frac{10}{1.2}, \frac{30}{1.2}, m = 1$</td>
</tr>
<tr>
<td>$R_C$</td>
<td>$8k\Omega$</td>
</tr>
<tr>
<td>$C_{C1}, C_{C2}, C_{CB}$</td>
<td>$3pF$</td>
</tr>
</tbody>
</table>

node. Since the bias transistor $M_{Nbias1}$ is the tail transistor for the differential amplifier, the compensation has almost no effect on it. Though the compensation induces any feedback current into the tail transistor $M_{Nbias1}$, the current mirror inside the differential amplifier cancels the effect of it.
Figure 3.8: Architecture of three-stage pseudo-class AB amplifier with inverted current buffer compensation.

Whereas, the bias transistor $M_{N2}$ creates an effect on node $V_2$, with the current induced by the feedback compensation. This creates a path from output node to internal node $V_2$ through compensation capacitor $C_{CB}$. The transistor $M_{N2}$ has inverting gain from its gate $V_{Bias}$ to drain $V_2$. Therefore, the transistor $M_{N2}$ is acting as a current buffer. The compensation appears as a capacitor in series with an inverted current buffer is connected between output node $V_{OUT}$ and intermediate node $V_2$. The architecture of the amplifier as shown in Fig 3.8 and the compensation is highlighted. Since the compensation capacitor is connected to a diode connected bias transistor $M_{bias}$, the input resistance of the current buffer must be $\frac{1}{g_{M_{bias}}}$.
3.3.2 Small-Signal Model

The small signal model of the amplifier with proposed inverted current buffer compensation is shown in Fig. 3.9. The transconductance of the first stage differential amplifier is denoted as $g_{M1}$ and the next stages are $g_{M2}$ and $g_{M3}$ respectively. The transconductance of feed-forward path is denoted as $g_{M3,F}$ and the current buffer in the compensation is denoted as $g_{MB}$. The resistance and capacitance at each internal output nodes are denoted as $R_1||C_1$, $R_2||C_2$ and $R_{OUT}||C_{OUT}$ respectively.

![Small-signal model of three-stage pseudo-class AB amplifier with inverted current buffer compensation.](image)

The dominant pole is mainly defined by the capacitance of main reverse nested Miller compensation $C_{C1}$, output resistance of first node $V_1$ and the gain of amplifier stages that covered by the main compensation. The equations of all the poles and zeros are tabulated in Table. 3.6. The inverted current-buffer compensation inserts a LHP zero without disturbing the other non-dominant poles and zeros. The second pole depends on the output capacitance and therefore it may limit the driving capability of the amplifier. Unlike the amplifier discussed before, the third non-dominant pole of amplifier with inverted current buffer compensation depend on compensation capacitors and resistors, but not on output capacitor. The two non-dominant poles are almost cancelled by the first two left
half plane (LHP) zeros created by the compensation. Therefore the amplifier is approximated as a two poles and one zero system. The LHP zero may be located just before or after high frequency non-dominant LHP pole depending on value of output capacitor. Though the second pole is dependent on the output capacitor, the three LHP zeros make the amplifier stable for a wide range of capacitive loads. The last pole is located at very high frequencies beyond the unity gain frequency, therefore the effect if it is neglected.

Table 3.6: Equations of Poles and Zeros of Amplifier with Inverted Current Buffer Compensation

<table>
<thead>
<tr>
<th>Poles</th>
<th>Zeros</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\omega_{P1} = \frac{1}{g_{M2}R_2g_{M3}R_{OUT}\cdot R_1\cdot C_1}$</td>
<td>$\omega_{Z1} = \frac{1}{R_C(C_{C1}+C_{C2})}$</td>
</tr>
<tr>
<td>$\omega_{P2} = \frac{g_{M2}C_{C1}}{C_{C2}C_{OUT}}$</td>
<td>$\omega_{Z2} = \frac{g_{M2}g_{M3}(C_{C1}+C_{C2})}{(g_{M2}+g_{Mf})C_{C1}C_{C2}}$</td>
</tr>
<tr>
<td>$\omega_{P3} = \frac{g_{M2}}{C_{C2}}$</td>
<td>$\omega_{Z3} = \frac{g_{Mbias}}{C_{CB}}$</td>
</tr>
<tr>
<td>$\omega_{P4} = \frac{R_1(g_{M2}C_{CB}+g_{Mbias}C_{C1})}{C_{CB}\cdot C_{C1}(R_1+R_C)}$</td>
<td></td>
</tr>
</tbody>
</table>

3.4 Simulation Results Compared with Inverted Current-Buffer Compensation

All the pseudo-class AB amplifiers and pseudo-class AB amplifier with inverted current-buffer compensation is designed and simulated in AMI 0.5\(\mu\)m process. The DC, AC and transient simulations are done and the outputs are shown in the next subsections. The results of I-I-N pseudo-class AB amplifier with inverted current-buffer compensation is compared with the results of I-I-N and I-N-I pseudo-class AB amplifier without inverted current-buffer compensation and the results are summarized in Table. 3.7.
Figure 3.10: AC analysis test bench of three-stage pseudo-class AB amplifiers without and with inverting current-buffer compensation.

Figure 3.11: Frequency plot of I-I-N three-stage pseudo-class AB amplifier.
Figure 3.12: Frequency plot of I-N-I three-stage pseudo-class AB amplifier.

Figure 3.13: Frequency plot of I-I-N three-stage pseudo-class AB amplifier with inverted current-buffer compensation.
3.4.1 AC Analysis

The frequency analysis of the amplifiers are done by breaking the loop of the amplifier with large resistor as shown in Fig. 3.10. The test bench has a AC input source with ac magnitude is set to 1 and the phase is set to 180°, such that the phase plot starts from 0°. AC simulation are done for different output loads of 100pF||10kΩ, 200pF||1MΩ, and 25pF||1kΩ. The locations of poles and zeros from the magnitude and phase plots are analysed and compared with the theoretical locations and they are nearly close values. Stability metrics such as, phase margin, gain margin and bandwidth are used to compare different designs.

The frequency plots of I-I-N pseudo-class AB amplifier, I-N-I pseudo-class AB amplifier, and I-I-N pseudo-class AB amplifier with inverted current-buffer compensation are shown in Fig. 3.11, Fig. 3.12 and Fig. 3.13 respectively.

![Transistor Amplifier Diagram](image)

Figure 3.14: Transient analysis test bench in non-inverting configuration.

3.4.2 Transient Analysis

The time analysis is done using transient analysis. The amplifier is tested as inverting configuration for rail-to-rail output swing. Two resistors of 200kΩ are
Figure 3.15: Transient output of I-I-N three-stage pseudo-class AB amplifier.

Figure 3.16: Transient output of I-N-I three-stage pseudo-class AB amplifier.
used to have an unity gain to the amplifier. The positive terminal is connected to ground and a 100kHz pulse signal is given as the input. The analysis is done for a loads of 100pF||1kΩ, 200pF||1MΩ, and 25pF||1kΩ and the waveforms are plotted. The metrics such as, slew rate and settling times are computed and used for comparing different designs.

The transient simulation outputs of I-I-N pseudo-class AB amplifier, I-N-I pseudo-class AB amplifier, and I-I-N pseudo-class AB amplifier with inverted current-buffer compensation are shown in Fig. 3.15, Fig. 3.16 and Fig. 3.17 respectively.

### 3.4.3 Power-Supply Rejection Ratio

Power-supply rejection ratio (PSRR) is used to find the attenuation of the noise from the power-supply by the amplifier. The test bench for finding
Figure 3.18: Test bench for finding PSRR.

Figure 3.19: Frequency plot of PSRR with and without inverted current-buffer compensation.
Table 3.7: Simulated Results

<table>
<thead>
<tr>
<th></th>
<th>I-I-N Pseudo-Class AB</th>
<th>I-N-I Pseudo-Class AB</th>
<th>I-I-N Pseudo-Class AB with CCB</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power supply</td>
<td>±1.25V</td>
<td>±1.25V</td>
<td>±1.25V</td>
</tr>
<tr>
<td>Dc gain</td>
<td>86dB</td>
<td>86.9dB</td>
<td>83dB</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>3.82MHz</td>
<td>4.53MHz</td>
<td>5.4MHz</td>
</tr>
<tr>
<td>Phase margin</td>
<td>56.2°</td>
<td>58°</td>
<td>56.7°</td>
</tr>
<tr>
<td>Gain margin</td>
<td>40dB</td>
<td>26dB</td>
<td>26dB</td>
</tr>
<tr>
<td>$R_{OUT}$</td>
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<tr>
<td>Total $C_C$</td>
<td>15pF</td>
<td>14.5pF</td>
<td>9pF</td>
</tr>
<tr>
<td>$SR + /SR − (V/µs)$</td>
<td>2.95/1.66</td>
<td>4.25/2.75</td>
<td>3.85/2.24</td>
</tr>
<tr>
<td>PSRR @1kHz</td>
<td>72.9dB</td>
<td>72.4dB</td>
<td>79.3dB</td>
</tr>
<tr>
<td>PSRR @10kHz</td>
<td>53.6dB</td>
<td>53.1dB</td>
<td>61.0dB</td>
</tr>
<tr>
<td>PSRR @100kHz</td>
<td>33.6dB</td>
<td>32.9dB</td>
<td>41.2dB</td>
</tr>
</tbody>
</table>

PSRR is shown in Fig. 3.18. The inputs of amplifier in inverting configuration is connected to ground and a ac sinusoidal signal source with 100mV$_{PP}$ is connected in series with the dc power-supply. The frequency of the ac signal is varied to calculate PSRR at different frequencies. The RMS voltage of the output to the RMS voltage of the input power supply gives the PSRR. Practically, the average
voltage is subtracted from the RMS voltage. The equation of PSRR is

\[ PSRR^+ = 20\log \left( \frac{V_{OUT,rms} - V_{OUT,Avg}}{V_{DD,rms} - V_{DD,Avg}} \right). \]  (3.3)

The PSRR is calculated at 1kHz, 10kHz and 100kHz frequencies for all the pseudo-class AB amplifiers and summarized in Table 3.7. The frequency plot of PSRR for pseudo-class AB without and with inverted current-buffer compensation is shown in Fig. 3.19.

The goal of the project is to convert the pseudo-class AB amplifier to a true class AB amplifiers. The I-N-I pseudo-class AB amplifier is converted to a true class AB amplifier by adding cascoded transistors and implemented inverted current buffer compensation to improve the stability. The I-N-I class AB amplifier is discussed in the next section.

3.5 I-N-I Three-stage Class AB Amplifier

The I-N-I pseudo-class AB amplifier shown in Fig. 3.4 is converted to a true class AB amplifier as shown in Fig. 3.20. The pseudo class-AB amplifier delivers a huge sinking current with low quiescent current and huge sourcing current with a huge quiescent current. When the amplifier has huge sourcing current, then the PMOS transistor of the second stage also has huge current. To avoid that huge current in the second stage, cascoded transistors are used in the mirror and made it a cascoded current mirror as shown in Fig. 3.20. The bias voltage \( V_{bp} \) for the PMOS bias transistor \( M_{P2,2} \) in second stage non-inverting common-source amplifier is generated by \( M_{Pbias} \) diode connected transistor as shown in Fig. 3.4. For this class AB amplifier, the bias voltage \( V_{bp} \) is generated by the diode connected transistor \( M_{P1,1} \) of the first stage differential amplifier as shown in Fig. 3.20.
Figure 3.20: Schematic of three-stage class AB amplifier.

Table 3.8: Dimensions of transistors of I-N-I Class AB Amplifier

<table>
<thead>
<tr>
<th>I-N-I class-AB</th>
<th>( \frac{10}{1.2}, m = 2 )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( M_{N1,1}, M_{N1,2}, M_{N2,1}, M_{N2,2}, M_{Ncas1}, M_{Ncas2} )</td>
<td>( \frac{30}{1.2}, m = 2 )</td>
</tr>
<tr>
<td>( M_{P1,1}, M_{P1,2}, M_{P2,1}, M_{P2,2} )</td>
<td>( \frac{10}{1.2}, \frac{30}{1.2}, m = 8 )</td>
</tr>
<tr>
<td>( M_{Nbias1} )</td>
<td>( \frac{10}{1.2}, m = 4 )</td>
</tr>
<tr>
<td>( M_{Nbias1}, M_{Ncas} )</td>
<td>( \frac{10}{1.2}, m = 1 )</td>
</tr>
<tr>
<td>( R_{CB} )</td>
<td>5kΩ</td>
</tr>
<tr>
<td>( C_{CB} )</td>
<td>4pF</td>
</tr>
</tbody>
</table>

3.5.1 Operation

As the input voltage \( V_{IN+} \) increases, the voltage at node \( V_1 \) decreases and increases current through \( M_{P2,1} \) transistor. Since, the feed-forward common-source path is formed between \( V_1 \) and output node, the current through the output transistor increases. The reduction in the voltage at node \( V_1 \) results in the increase
the current through $M_{P2,1}$. In the pseudo-class AB amplifier shown in Fig. 3.4, the current through the second stage is not limited to the bias current. But in this class AB amplifier, the current is limited by the cascoded transistor $M_{NCAS1}$ and therefore the voltage at the gate of current mirror increases and in turn decreases the voltage at node $V_2$. This turns off the output NMOS transistor $M_{N3}$. Since all the internal stage currents of the amplifier are limited by the bias current, the quiescent current is very low when there is a huge sourcing current.

As the input voltage $V_{IN-}$ increases, the voltage at node $V_1$ also increases. This turns off the PMOS transistor $M_{P2,1}$ and the feed-forward PMOS transistor $M_{PF}$. As the voltage at node $V_1$ increases, the voltage at node $V_2$ also increases. This increases the sinking current through the output NMOS transistor $M_{N4}$. Similar to the pseudo-class AB amplifier shown in Fig. 3.4, all the internal stage currents of the amplifier are limited by the bias current, the quiescent current is very low when there is a huge sinking current.

This explains the push-pull action of the amplifier when $V_{IN+}$ and $V_{IN-}$ increases respectively. The maximum sourcing current through $M_{PF}$ is limited by the common-mode input voltage applied to $V_{IN+}$ and $V_{IN-}$. On the other hand, the maximum sinking current through $M_{N3}$ is only limited by the supply voltage. This confirms the true class AB characterization of I-N-I three-stage class AB amplifier.

### 3.5.2 Nested Inverted Current-Buffer Compensation

The I-N-I pseudo-class AB amplifier is compensated with nested Miller compensation and is stable for wide range of capacitive and resistive loads. The class AB amplifier shown in Fig. 3.20 is compensated with the inverted current-buffer compensation and nested-miller compensation. The inverted current-buffer compensation $C_{CB}$ and $R_{CB}$ is connected from node $V_2$ to the gate of the current
mirror in the first stage differential amplifier. This help in forming two inverted current-buffers, one is formed by $M_{P1,2}$ transistor and the other is formed by $M_{P2,2}$ transistor. Therefore the compensation looks like a capacitor in series with resistor and current-buffer in series to the node $V_1$ and a current-buffer to node $V_2$. It is clearly observed in the architecture of class AB amplifier as shown in Fig. 3.21. Therefore the compensation is called as nested inverted current-buffer compensation. This increases the stability and bandwidth of the class AB amplifier.

3.5.3 Small-Signal Analysis

The small signal model of the I-N-I class AB amplifier with inverted current buffer compensation is shown in Fig. 3.22. The transconductance of the first stage differential amplifier is denoted as $g_{M1}$ and the next stages are $g_{M2}$ and
The transconductance of feed-forward path is denoted as $g_{MF}$ and the current buffer in the compensation is denoted as $g_{Mx}$. The resistance and capacitance at each internal output nodes are denoted as $R_1||C_1, R_2||C_2$ and $R_{OUT}||C_{OUT}$ respectively. The gain of the amplifier is same as the discussed amplifier given by

$$Gain = g_{M1}R_1 \cdot (g_{M2}R_2 \cdot g_{M3}R_{OUT} + g_{MF}R_{OUT}).$$  \hspace{1cm} (3.4)$$

The amplifier has four poles; the compensation capacitance $C_{CB}$ creates the dominant pole. The effect of the non-dominant pole can be nullified by proper placement of the LHP zero $\omega_{Z_1}$ created by the inverted current-buffer compensation. The equation of all poles and zeros are mentioned in Table \[3.9\]. The equation of second pole is dependent on output resistor and capacitor. If the output capacitor is too small, then the second pole moves to higher frequencies. If the capacitor is moderate, then the effect of pole is nullified by proper placement of LHP zero. Therefore, the class AB amplifier is stable for low and moderate output capacitance values. If the capacitor is too large, then the poles moves to lower frequencies and effects the stability, phase margin and gain margin of the amplifier.
Similar to the output capacitance, the range of output resistance also effects the movement of poles and zeros. If the output resistance $R_{OUT}$ is too small, then the second pole moves to higher frequencies. If $R_{OUT}$ is moderate then the second pole moves to moderate frequency and its effect is cancelled by proper placement of LHP zero. If $R_{OUT}$ is too huge, then the second pole moves to lower frequencies and effects the stability of the amplifier.

The combination of output capacitance and resistance effects the stability of the class AB amplifier. For large output capacitance values, the amplifier is stable for with low output resistor values. For small output capacitor, the amplifier is stable for high output resistor.

The last two poles and last zero are at very high frequencies. The last pole can be cancelled by proper placement of the lase zero. Therefore, the effect of that pole and zero has almost no effect on the stability of the amplifier. The I-N-I class AB amplifier overcomes the drawback of the pseudo-class AB amplifiers. But, the class AB amplifier has slightly higher quiescent current with sourcing current than the quiescent current with sinking current. This is because of the presence of cascoded current mirror that has four times the bias current through
output transistor when the gate voltage goes close to negative rail voltage. This drawback is overcome by the proposed class AB amplifier discussed in next section.

3.6 Proposed Three-stage True Class AB Amplifier

The schematic of the proposed three-stage class AB amplifier is shown in Fig. 3.23. The first stage is a differential amplifier. Inverting common-source amplifiers make up the next stages. The first two inverting common-source amplifiers $M_{P2}/M_{N2}$ and $M_{P3}/M_{N3}$ are combined with gate-drain feedback to behave as a single non-inverting common-source stage. The output stage is formed by the inverting common-source amplifiers $M_{N4}$ and $M_{PF}$. The common-source amplifier $M_{PF}$ is the feed-forward path from $V_1$ node to the output node. All internal transistors have low quiescent current whereas the output stage has huge sourcing and sinking current capability. This confirms the true class AB operation of the output stage.

![Figure 3.23: Schematic of proposed three-stage class AB amplifier.](image)

The proposed class AB amplifier employs both nested Miller compensation and reverse-nested Miller compensation techniques for stability. The main compensation network $C_{C1}$ and $R_{C1}$ with $C_{C2}$ and $R_{C2}$ forms the nested Miller
compensation and $C_{C1}$ and $R_{C1}$ with $C_{C3}$ and $R_{C3}$ forms the reverse-nested Miller compensation network. The dimensions of all transistors, capacitors and resistors are given in Table 3.10. The nested and reverse nested Miller compensation including the gate-drain feedback resistance helps in stabilizing the amplifier for a wide range of capacitive and resistive loads.

Table 3.10: Dimensions of transistors Proposed Class AB Amplifier

<table>
<thead>
<tr>
<th>Proposed class-AB</th>
<th>$M_{N1,1}, M_{N1,2}, M_{N2}, M_{N3}$</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$10 \frac{1}{2}, m = 2$</td>
</tr>
<tr>
<td>$M_{P1,1}, M_{P1,2}, M_{P2}, M_{P3}$</td>
<td>$30 \frac{1}{2}, m = 2$</td>
</tr>
<tr>
<td>$M_{N4}$ &amp; $M_{PF}$</td>
<td>$10 \frac{1}{2} &amp; 30 \frac{1}{2}, m = 8$</td>
</tr>
<tr>
<td>$M_{Nbias}$</td>
<td>$10 \frac{1}{2}, m = 4$</td>
</tr>
<tr>
<td>$M_{Nbias}$</td>
<td>$10 \frac{1}{2}, m = 1$</td>
</tr>
<tr>
<td>$R_{C1}, R_{C2}, R_{C3}, R_{C4}$</td>
<td>$1k\Omega, 20k\Omega, 12k\Omega, 100k\Omega$</td>
</tr>
<tr>
<td>$C_{C1}, C_{C2}, C_{C3}$</td>
<td>5pF, 2pF, 5pF</td>
</tr>
</tbody>
</table>

3.6.1 Gate-Drain Feedback

The overall gain and effective the number of stages of the proposed class AB amplifier are decreased by introducing the gate-drain feedback resistor $R_{C4}$ across the third stage. The presence of $R_{C4}$ nullifies the gain of the first common-source amplifier and helps in moving its dominant pole to high frequencies. According to the Miller effect, the resistor across the amplifier splits between the input and the output. Since the gain of the amplifier is inverting, the resistance at the input node is reduced by the gain of the amplifier and is approximately equal to $\frac{R_{C4}}{1 + g_{MP3}}$. The resistance at the output node is equal to $R_{C4}(1 + \frac{1}{g_{MP3}})$ which is approximately equal to $R_{C4}$. Therefore, the gain of second stage is $(g_{M2} \frac{R_{C4}}{g_{MP3} R_{C4}})$
and the gain of next stage is \((g_{MP3} \cdot R_{C4})\). Therefore the combined cascaded gain to these two stages is \((g_{M2} \cdot R_{C4})\) showing the cancellation of first common-source amplifier.

The value of gate-drain feedback resistance \(R_{C4}\) is chosen in such a way that the voltage drop across \(R_{C4}\) is nearly equal to the supply voltage. Using mathematical and simulated results, \(R_{C4}\) is computed as 100k\(\Omega\) whereas the current through \(M_{N3}\) transistor is 20\(\mu\)A.

![Architecture of the proposed three-stage class AB amplifier.](image)

**Figure 3.24:** Architecture of the proposed three-stage class AB amplifier.

### 3.6.2 Operation

As the input \(V_{in+}\) increases the current through the \(M_{N1,2}\) increases results in the decrement of voltage at node \(V_1\). Therefore the current through \(M_{P2}\) and \(M_{PF}\) increases. Since the transistor \(M_{N2}\) can source only bias current, the voltage at node \(V_2\) increases. The current through \(M_{P3}\) is limited to the sum of \(I_{bias2}\) and \(I_{bias3}\), resulting in a decrease in the voltage at node \(V_3\). This turns off the final
stage NMOS transistor $M_{N4}$. The PMOS transistor $M_{PF}$ forms a feed-forward path from the intermediate node $V_1$ to the output. Therefore the amplifier delivers source current if $V_{IN+}$ increases.

Conversely, if $V_{IN-}$ increases then the current sinking through the NMOS transistor $M_{N4}$ increases. In this case the voltage at node $V_1$ increases, turning off PMOS transistor $M_{PF}$. This explains the push-pull action of the amplifier. The maximum sourcing current through $M_{PF}$ is limited by the common-mode input voltage applied to $V_{IN+}$ and $V_{IN-}$. On the other hand, the maximum sinking current through $M_{N4}$ is only limited by the supply voltage.

### 3.6.3 Nullified Effect of Inverted Current-Buffer Compensation

The inverted current-buffer compensation technique is used to improve the stability and bandwidth. To implement this compensation, the amplifier must have atleast one bias transistor. The proposed three-stage class AB amplifier has three bias transistors; if the compensation is applied to the amplifier, then the stability and the bandwidth will increase. But the analysis proved that the effect of inverted current-buffer compensation is nullified.

Assume that the compensation is implemented in the proposed class AB amplifier. A capacitor is connected between the output node to the bias node. Let the compensation induces an extra current through bias transistors. The current through the $M_{Bias}$ transistor, which is the tail transistor of differential amplifier and is compensated by the differential pair transistors. The extra current through the $M_{N2}$ transistor decreases the voltage at node $V_2$. Because of the common-source amplifier formed by $M_{P3}$ transistor, the reduction in the $V_2$ voltage increases the voltage at node $V_3$. But the extra current through the $M_{N3}$ transistor induced by the inverted current-buffer compensation decreases the voltage at node
V_3 and balances the effect. This explains the nullified effect of inverted current-buffer compensation.

Figure 3.25: Small-signal model of the proposed three-stage class AB amplifier.

### 3.6.4 Small-Signal Analysis

The small signal model of the proposed class AB amplifier is shown in Fig. 3.25. The transconductance of the first stage differential amplifier is denoted as \( g_{M1} \) and the next stages are \( g_{M2} \), \( g_{M_{gd}} \) and \( g_{M4} \) respectively. The transconductance of feed-forward path is denoted as \( g_{M_F} \). The resistance and capacitance at each stage’s output nodes are denoted as \( R_1 || C_1 \), \( R_2 || C_2 \), \( R_3 || C_3 \) and \( R_{OUT} || C_{OUT} \). The gain of the class AB amplifier is the product of all the amplifier gains. With the gate-drain feedback resistance, the gain at node \( V_2 \) is nullified and therefore the total gain is given by

\[
Gain = g_{M1}R_1 \cdot g_{M2}R_{C4} \cdot g_{M4}R_{OUT}. \quad (3.5)
\]

The dominant pole is determined by the compensation capacitor \( C_{C1} \), the output resistance \( R_1 \) and the gain of amplifier stages covered by the main compensation. The equation of the dominant pole is given by

\[
\omega_{P1} = \frac{1}{g_{M2}R_{C4} \cdot g_{M4}R_{OUT} \cdot R_1 \cdot C_{C1}}. \quad (3.6)
\]
The next two non-dominant poles can be cancelled by the proper placement of first two left-half-plane (LHP) zeros created by the compensation. Therefore the amplifier is approximated as a two-pole and single-zero system. The LHP zero may be located just before or after high frequency non-dominant LHP poles, depending on value of output capacitor; therefore the amplifier is unconditionally stable. The effect of the last LHP pole can be nearly eliminated by adjusting the location of the third LHP zero.

The equations of all poles and zeros are summarized in Table 3.11. Unlike the pseudo-class AB amplifier, the intermediate non-dominant poles of the proposed class AB amplifier depend on the compensation capacitors and resistors, but not on the output capacitor. Therefore, the amplifier is stable for a wider range of load capacitance values. The stability for wide range of loads is limited by the last pole, which depends on the output capacitor and is generally located far beyond the unity gain frequency.

### Table 3.11: Equations of Poles and Zeros of Proposed Class AB Amplifier

<table>
<thead>
<tr>
<th></th>
<th>Poles</th>
<th>Zeros</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \omega_{P1} )</td>
<td>( \frac{1}{g_{m2}R_{C3}g_{m4}R_{OUT}R_{1}C_{1}} )</td>
<td>( \frac{1}{R_{C1}C_{1}C_{1}+R_{C2}C_{2}C_{2}+R_{C3}C_{3}} )</td>
</tr>
<tr>
<td>( \omega_{P2} )</td>
<td>( \frac{1}{R_{C2}C_{2}+R_{C3}C_{3}} )</td>
<td>( \frac{1}{R_{C1}C_{1}+R_{C2}C_{2}+R_{C3}C_{3}} )</td>
</tr>
<tr>
<td>( \omega_{P3} )</td>
<td>( \frac{R_{C2}C_{2}+R_{C3}C_{3}}{R_{C2}C_{2}R_{C3}C_{3}} )</td>
<td>( \frac{R_{C1}C_{1}C_{1}+R_{C2}C_{2}C_{2}+R_{C3}C_{3}C_{3}}{R_{C1}C_{1}C_{1}+R_{C2}C_{2}C_{2}+R_{C3}C_{3}C_{3}} )</td>
</tr>
<tr>
<td>( \omega_{P4} )</td>
<td>( \frac{g_{m3}R_{C2}g_{m4}R_{C3}}{R_{1}C_{OUT}} )</td>
<td>( \frac{1}{R_{C1}C_{1}C_{1}} + \frac{1}{R_{C2}C_{2}} + \frac{1}{R_{C3}C_{3}} )</td>
</tr>
</tbody>
</table>

3.7 Simulation Results Compared with the Proposed Class AB Amplifier

The proposed class AB amplifier is designed and simulated in AMI 0.5\( \mu \)m process. The DC, AC and transient analysis and simulations are done and the
outputs are shown in the next subsections. The results of proposed class AB amplifier is compared with the results of I-I-N and I-N-I pseudo-class AB amplifiers and the results are summarized in Table. 3.12.

3.7.1 DC Analysis

DC currents are very important to characterize the amplifier as a class AB or pseudo-class AB. DC analysis is used to plot the sourcing, sinking and quiescent currents. The test bench for DC simulation is shown in Fig. 3.26. DC source is given as the input to the amplifier in open-loop configuration and sweep the dc voltage from -30mV to 30mV. The currents at the output stage and the total quiescent currents are plotted. The dc currents of I-I-N, I-N-I pseudo-class AB, I-N-I class AB and proposed class AB amplifiers are shown in Fig. 3.27, Fig. 3.28, Fig. 3.29 and Fig. 3.30 respectively. For I-I-N pseudo-class AB amplifier, the quiescent current is low for huge sourcing current; as the sinking current increases, the quiescent current goes very high as shown in Fig. 3.27. Conversely, in I-N-I pseudo-class AB amplifier, the quiescent current increases with the sourcing current as shown in Fig. 3.28. These results prove that the two amplifiers are pseudo-class AB amplifiers.

Figure 3.26: DC analysis test bench of proposed three-stage class AB amplifier.
Figure 3.27: DC currents of I-I-N three-stage pseudo-class AB amplifier.

Figure 3.28: DC currents of I-N-I three-stage pseudo-class AB amplifier.
Figure 3.29: DC currents of I-N-I three-stage class AB amplifier.

Figure 3.30: DC currents of proposed three-stage class AB amplifier.
For I-N-I class AB amplifier, the quiescent current is very low for huge sinking current and slightly higher for huge sourcing current as shown in Fig. 3.29. The quiescent current is nearly constant even when the output current is increased. This result prove that the amplifier is a true class AB amplifier.

The proposed class AB amplifier has nearly constant quiescent current for huge sourcing and sinking currents as shown in Fig. 3.30. This result prove that the proposed amplifier is a true class AB amplifier.

![AC analysis test bench of proposed three-stage class AB amplifier.](image)

3.7.2 AC Analysis

The frequency analysis of the amplifiers are done by breaking the loop of the amplifier with large resistor as shown in Fig. 3.31. The test bench has a AC input source with ac magnitude is set to 1 and the phase is set to 180°, such that the phase plot starts from 0°. AC simulation are done for different output loads of 100pF∥10kΩ, 200pF∥1MΩ, and 25pF∥1kΩ. The locations of poles and zeros from the magnitude and phase plots are analysed and compared with the
Figure 3.32: Frequency plot of I-I-N three-stage class AB amplifier.

Figure 3.33: Frequency plot of I-N-I proposed class AB amplifier.
theoretical locations and they are nearly close values. Stability metrics such as, phase margin, gain margin and bandwidth are used to compare different designs.

The frequency plots of I-N-I class AB amplifier, and proposed class AB amplifier are shown in Fig. 3.32 and Fig. 3.33 respectively.

3.7.3 Transient Analysis

The time analysis is done using transient analysis. The amplifier is tested as inverting configuration for rail-to-rail output swing. Two resistors of 200kΩ are used to have an unity gain to the amplifier. The positive terminal is connected to ground and a 100kHz pulse signal is given as the input. The analysis is done for a loads of 100pF||10kΩ, 200pF||1MΩ, and 25pF||1kΩ and the waveforms are plotted. The metrics such as, slew rate and settling times are computed and used for comparing different designs. The transient simulation outputs of I-N-I class AB amplifier, and proposed class AB amplifier are shown in Fig. 3.35 and Fig. 3.36 respectively.

![Figure 3.34: Transient analysis test bench in non-inverting configuration of proposed three-stage class AB amplifier.](image)
Figure 3.35: Transient output of I-N-I three-stage class AB amplifier.

Figure 3.36: Transient output of proposed class AB amplifier.
<table>
<thead>
<tr>
<th>Table 3.12: Simulated Results</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
</tr>
<tr>
<td>---</td>
</tr>
<tr>
<td>Dc gain</td>
</tr>
<tr>
<td>Bandwidth</td>
</tr>
<tr>
<td>Phase margin</td>
</tr>
<tr>
<td>Gain margin</td>
</tr>
<tr>
<td>$R_{OUT}$</td>
</tr>
<tr>
<td>Total $C_C$</td>
</tr>
<tr>
<td>Power supply</td>
</tr>
<tr>
<td>$I_{SRC}/I_{SINK}$ at 1kΩ</td>
</tr>
<tr>
<td>$I_{Q,max}$ at 1kΩ</td>
</tr>
<tr>
<td>$I_{EFF}$ at 1kΩ</td>
</tr>
<tr>
<td>SR+/SR- (V/µs)</td>
</tr>
</tbody>
</table>
Chapter 4

EXPERIMENTAL RESULTS

The layout of all the amplifiers and the microscopic view of chip and the hardware results are discussed in this chapter.

4.1 Layout

The layout of all the amplifier are shown. The layout of I-I-N pseudo-class AB amplifier is shown in Fig. 4.1. The area of the amplifier is around $263 \times 191 \mu m^2$. It has a minimum output driving load capacitance of $10 \mu F$, which is also layed-out with the amplifier.

The layout of I-I-N pseudo-class AB with inverted current-buffer compensation is shown in Fig. A.2. The area of the amplifier is around $226 \times 183 \mu m^2$. It has a minimum output driving load capacitance of $10 \mu F$, which is also layed-out with the amplifier.

The layout of I-N-I pseudo-class AB amplifier is shown in Fig. 4.3. The area of the amplifier is around $173 \times 170 \mu m^2$.

The layout of proposed amplifier is shown in Fig. 4.4. The area of the amplifier is around $177 \times 167 \mu m^2$.

The layout of overall chip is shown in Fig. 4.5. The chip contains 12 circuits in which, each of the above four amplifiers are repeated thrice. Two sets of amplifiers are in open-loop configuration and one set of amplifiers are in closed-loop configuration with unity gain.
Figure 4.1: Layout of I-I-N pseudo-class AB amplifier.

Figure 4.2: Layout of I-I-N pseudo-class AB amplifier with inverted current-buffer compensation.
Figure 4.3: Layout of I-N-I pseudo-class AB amplifier.

Figure 4.4: Layout of proposed class AB amplifier.
4.2 Test apparatus

We used a power supply for supplying an voltage supply of ±1.25 and ground. A agilent 5400 function generator is used to generate a 100kHz pulse signal with a peak-to-peak voltage of 2.5V. A Hewlett Packard 54603B oscilloscope is used to observe the waveforms of transient analysis as described in the test procedure shown in APPENDIX A. Two agilent 34401A 6½ Digital Multimeter (DMM) are used for measuring output voltages, currents and quiescent currents.
4.3 Hardware Transient Result

Chip was fabricated in a 0.5µm 2P3M ONSEMI technology through MOSIS. The chip was tested with supply voltages ±1.25V and an input bias current of 10µA to all the amplifiers.

Transient measurements were performed for the amplifiers with the inverting configuration and unity-gain feedback. Two 200kΩ resistors were used in the negative feedback to achieve unity gain. The input is a 100kHz square wave with peak-to-peak voltage of 2.5V. All the amplifier was tested for a different combinations of load and three of the combination outputs are presented. The positive slew rate is measured as the slope of the rising edge from 10% to 90% of output peak-to-peak voltage and the negative slew rate is similar for falling edge.

4.3.1 I-I-N Three-Stage Pseudo-Class AB Amplifier

![3-Stage Pseudo Class-AB Amplifier](image)

Figure 4.6: Hardware transient output of I-I-N pseudo-class AB amplifier.
The measured slew rates of the I-I-N three-stage pseudo-class AB amplifier for standard load of $10k\Omega || 100pF$ are $2.86V/\mu s$ and $1.74V/\mu s$. Since gains of the feed-forward path and the three-stage path are different, the settling time for the rising edge is higher than the settling time for the falling edge.

4.3.2 I-I-N Three-Stage Pseudo-Class AB Amplifier with Inverting Current-Buffer Compensation

The measured slew rates of the I-I-N three-stage pseudo-class AB amplifier with inverting current-buffer compensation for standard load of $10k\Omega || 100pF$ are $2.04V/\mu s$ and $1.54V/\mu s$. Since gains of the feed-forward path and the three-stage path are different, the settling time for the rising edge is higher than the settling time for the falling edge.
4.3.3 I-N-I Three-Stage Pseudo-Class AB Amplifier

The measured slew rates of the I-N-I three-stage pseudo-class AB amplifier for standard load of 10kΩ||100pF are 1.82V/µs and 2.66V/µs. Since gains of the feed-forward path and the three-stage path are different, the settling time for the rising edge is higher than the settling time for the falling edge.

4.3.4 Proposed Three-Stage True Class AB Amplifier

The measured slew rates of the class AB amplifier for standard load of 10kΩ||100pF are 3.13V/µs and 1.7V/µs. Since gains of the feed-forward path and the three-stage path are different, the settling time for the rising edge is higher than the settling time for the falling edge.

4.4 Measurement Results

The dc sourcing, sinking and quiescent currents of all amplifiers are measured and the results are tabulated in Table 2.1. The measured output currents
of all the amplifiers are approximately 1.10mA sourcing from positive rail and 1.12mA from negative rail for 1kΩ resistive load when connected to ±1.25V power supply.

The maximum quiescent current to the negative power supply of the I-I-N and I-N-I pseudo-class AB amplifiers are huge for the huge sinking and sourcing currents respectively. The maximum quiescent current of proposed class AB amplifier is nearly constant irrespective of the huge sourcing and sinking currents. The current efficiency is calculated as the maximum output current to the sum of maximum output current and maximum quiescent current. The measured maximum output current, maximum quiescent current, current efficiency and slew rates are summarized in Table 1.
<table>
<thead>
<tr>
<th></th>
<th>I-I-N Pseudo-Class AB</th>
<th>I-I-N with CCB</th>
<th>I-N-I Pseudo-Class AB</th>
<th>Proposed Class AB</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power supply</td>
<td>±1.25V</td>
<td>±1.25V</td>
<td>±1.25V</td>
<td>±1.25V</td>
</tr>
<tr>
<td>$I_{SRC}/I_{SINK}$ at 1kΩ</td>
<td>1.08mA/1.10mA</td>
<td>1.08mA/1.10mA</td>
<td>1.12mA/1.10mA</td>
<td>1.12mA/1.16mA</td>
</tr>
<tr>
<td>$I_{Q,max}$ at 1kΩ</td>
<td>138µA/300µA</td>
<td>140µA/300µA</td>
<td>483µA/95µA</td>
<td>95µA/98µA</td>
</tr>
<tr>
<td>$I_{EFF}$ at 1kΩ</td>
<td>79%</td>
<td>79%</td>
<td>69.5%</td>
<td>92%</td>
</tr>
<tr>
<td>PSRR @ 1kHz</td>
<td>78.2dB</td>
<td>-</td>
<td>-</td>
<td>72.5dB</td>
</tr>
<tr>
<td>PSRR @ 10kHz</td>
<td>58.7dB</td>
<td>-</td>
<td>-</td>
<td>64.0dB</td>
</tr>
<tr>
<td>PSRR @ 100kHz</td>
<td>31.3dB</td>
<td>-</td>
<td>-</td>
<td>36.3dB</td>
</tr>
<tr>
<td>$SR$ / $SR$ (V/µs)</td>
<td>2.86/1.74</td>
<td>1.84/1.54</td>
<td>1.82/2.66</td>
<td>3.13/1.7</td>
</tr>
</tbody>
</table>
Chapter 5

DISCUSSION AND CONCLUSION

The simulation and measurement results of proposed class AB amplifier is com-
pared with the pseudo-class AB amplifiers and are tabulated. The design of
proposed class AB amplifier is similar to the pseudo-class AB amplifier in low
supply-voltage, simple biasing, low transistor-count, wide output-swing and low
bias current. The results of class AB amplifier are comparable with the pseudo-
class AB amplifier in gain, phase margin, gain margin, and maximum output
current. But the proposed amplifier realizes the high current efficiency with low
quiescent current, increased in bandwidth, and decreased compensation capaci-
tance.

The class AB amplifier is stable for 500Ω of load resistance and has sourcing
and sinking currents of 2.1mA and 1.9mA. The amplifiers are also tested with a
power supply of ±2.0V to deliver a current of 1.98mA and 3.27mA of sourcing
currents and 1.97mA and 3.36mA of sinking currents for 1kΩ and 500Ω resistive
loads, respectively.

Finally, two different three-stage pseudo-class AB amplifiers are converted
to two different three-stage class AB amplifiers. The proposed class AB amplifier
has a higher current-efficiency and a higher bandwidth than the pseudo-class AB
amplifier. The poles and zeros of all the amplifiers are theoretically computed,
analysed and presented in the report. All the amplifiers are fabricated and the
results analysed in the simulation are verified by the experimental results.
5.0.1 Issues

The fabricated chip has 12 circuits of four different types. The four circuits are I-I-N pseudo-class AB amplifier, I-N-I pseudo-class AB amplifier, I-I-N pseudo-class AB with inverted current-buffer compensation and proposed class AB amplifier. Each of these circuits are repeated three times, two of them are open-loop configuration and the third is of closed-loop configuration. The circuits of the same kind have common bias pin. Therefore, we cannot be able to measure quiescent current correctly. Therefore, we approximated the quiescent current by subtracting the bias current of other two amplifiers.

And the other issue is that the internal nodes of multi-stage amplifiers should be turned off. Otherwise, the nodes will be floating and may draw some current through the transistors.

The I-I-N pseudo-class AB amplifier has a huge quiescent current when the sinking current is huge. In a simulation, the quiescent current is approximately 900\(\mu\)A for a sinking current of 1.16mA. But the hardware results show that the quiescent current is approximately 320\(\mu\)A for a sinking current of 1.15mA. We were not able to find the reason because of a lack of time.

5.0.2 Anomalies

In this thesis we did not discuss the cross-over distortion. The pseudo-class AB amplifiers and class AB amplifiers has a huge distortion. Our major goal is to convert the widely-used pseudo-class AB amplifier to a true class AB amplifier. Therefore, we did not consider the distortion of the amplifier.

5.0.3 Future Work

The proposed class AB amplifier is a true class AB amplifier. This is designed as the general purpose amplifier. Therefore, the amplifier can be improved as an application oriented amplifier such as audio amplifier, power amplifier, mo-
tor driver and LCD & LED driver. We need to deal with the distortion of the class AB amplifiers.

The I-N-I class AB amplifier is working perfectly and the amplifier is not fabricated. We did not complete the whole analysis on this class AB amplifier. The I-N-I class AB amplifier is compensated with single inverted current-buffer compensation which appears as nested inverted current-buffer compensation. The amplifier is stable for very low resistive load of range $10\Omega-1k\Omega$. Therefore, this amplifier can be implemented as an audio amplifier for a resistive load of $16\Omega$. 
APPENDICES
APPENDIX A

Test Document
A.1 Supply Voltages and Currents

\[ V_{DD} = 1.25V \]
\[ V_{SS} = -1.25V \]
\[ I_{Bias} = 10 \mu A \]

A.2 Procedure

1. Connect \( V_{DD} \) (pin16) and \( V_{SS} \) (pin36) and check whether the chip is good or fired up.

2. Connect \( V_{DD} \) (Pin16) to \( V_{DD1} \) (pin4) which is power supply to all the amplifiers that are on top

3. Attach bias resistor to each amplifier separately

- Three-Stage I-I-N Pseudo-Class AB Amplifier

The bias current is 10\( \mu A \), the supply voltage \( V_{DD} \) is 1.25V and \( V_{bn1} \) is -324.1mV. Therefore the bias resistor is given by

\[
R = \frac{V_{DD} - V_{bn1}}{I_{Bias}} = 157.4k\Omega \quad (1)
\]

Since it is supplying current to three amplifiers, the resistance should be three times less than the calculated.

\[
R = 53k\Omega \ [Sincethreeamplifiers] \quad (2)
\]

Connect \( V_{bn1} \) (pin8) to one end of the bias resistor and other end of resistor is connected to \( V_{DD} \) (Pin16)
<table>
<thead>
<tr>
<th>Pin #</th>
<th>Name</th>
<th>Pad type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>$V_{OUT11}$</td>
<td>Protected</td>
<td>Output of 3-stage class AB amplifier which is connected as a voltage follower</td>
</tr>
<tr>
<td>2</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>3</td>
<td>$V_{IN3+}$</td>
<td>Protected</td>
<td>Input to positive terminal of all amplifiers that are connected as voltage followers</td>
</tr>
<tr>
<td>4</td>
<td>$V_{DD1}$</td>
<td>Protected</td>
<td>Vdd supply to all the amplifiers that are on the top</td>
</tr>
<tr>
<td>5</td>
<td>$V_{IN1+}$</td>
<td>Protected</td>
<td>Input to the positive terminal of all the amplifiers connected on top</td>
</tr>
<tr>
<td>6</td>
<td>$V_{IN1,1-}$</td>
<td>Protected</td>
<td>Input to the negative terminal of the 3-stage pseudo class-AB amplifier on the top</td>
</tr>
<tr>
<td>7</td>
<td>$V_{OUT1}$</td>
<td>Protected</td>
<td>Output of the 3-stage pseudo class-AB amplifier on the top</td>
</tr>
<tr>
<td>8</td>
<td>$V_{bn}$</td>
<td>Protected</td>
<td>Bias pin for the NMOS to all the 3-stage pseudo class-AB amplifiers</td>
</tr>
<tr>
<td>9</td>
<td>$V_{OUT3}$</td>
<td>Protected</td>
<td>Output of 3-stage class-AB amplifier on the top</td>
</tr>
<tr>
<td>10</td>
<td>$V_{bp3}$</td>
<td>Protected</td>
<td>Bias pin for PMOS to all the 3-stage class-AB amplifiers</td>
</tr>
<tr>
<td>11</td>
<td>$V_{IN1,3-}$</td>
<td>Protected</td>
<td>Input to the negative terminal of 3-stage class-AB amplifier on the top</td>
</tr>
<tr>
<td>12</td>
<td>$V_{OUT4}$</td>
<td>Protected</td>
<td>Output of 4-stage class-AB amplifier on the top</td>
</tr>
<tr>
<td>13</td>
<td>$V_{IN1,4-}$</td>
<td>Protected</td>
<td>Input to the negative terminal of the 4-stage class-AB amplifier on the top</td>
</tr>
<tr>
<td>14</td>
<td>$V_{OUT2}$</td>
<td>Protected</td>
<td>Output of 3-stage pseudo class-AB amplifier with bias-line compensation on the top</td>
</tr>
<tr>
<td>15</td>
<td>$V_{IN1,2-}$</td>
<td>Protected</td>
<td>Input to the negative terminal of the pseudo class-AB with $C_{CB}$ on top</td>
</tr>
<tr>
<td>16</td>
<td>Global $V_{DD}$</td>
<td>+ve</td>
<td>-</td>
</tr>
<tr>
<td>17</td>
<td>$V_{SS}$</td>
<td>Protected</td>
<td>-</td>
</tr>
<tr>
<td>18</td>
<td>$V_{bn2}$</td>
<td>Protected</td>
<td>Bias pin for NMOS to all 3-stage pseudo class-AB amplifiers with $C_{CB}$</td>
</tr>
<tr>
<td>19</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>20</td>
<td>$V_{OUT12}$</td>
<td>Protected</td>
<td>Output of 4-stage class-AB amplifier connected as voltage follower</td>
</tr>
<tr>
<td>Pin #</td>
<td>Name</td>
<td>Pad type</td>
<td>Description</td>
</tr>
<tr>
<td>-------</td>
<td>-----------</td>
<td>----------</td>
<td>-----------------------------------------------------------------------------</td>
</tr>
<tr>
<td>21</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>22</td>
<td>V_{OUT10}</td>
<td>Protected</td>
<td>Output of 3-stage pseudo class-AB amplifier with $C_{CB}$ connected as voltage follower</td>
</tr>
<tr>
<td>23</td>
<td>V_{DD3}</td>
<td>Protected</td>
<td>Vdd supply to all the 4 amplifiers that are connected as voltage followers</td>
</tr>
<tr>
<td>24</td>
<td>V_{SS}</td>
<td>Protected</td>
<td>-</td>
</tr>
<tr>
<td>25</td>
<td>V_{IN2+}</td>
<td>Protected</td>
<td>Input to the positive terminal of all the four amplifiers that are at the bottom</td>
</tr>
<tr>
<td>26</td>
<td>V_{IN2,2-}</td>
<td>Protected</td>
<td>Input to the negative terminal of 3-stage pseudo class-AB amplifier with $C_{CB}$ at bottom</td>
</tr>
<tr>
<td>27</td>
<td>V_{OUT6}</td>
<td>Protected</td>
<td>Output of 3-stage pseudo class-AB amplifier with $C_{CB}$ at the bottom</td>
</tr>
<tr>
<td>28</td>
<td>V_{IN2,4-}</td>
<td>Protected</td>
<td>Input to the negative terminal of 4-stage class-AB amplifier at the bottom</td>
</tr>
<tr>
<td>29</td>
<td>V_{OUT8}</td>
<td>Protected</td>
<td>Output of 4-stage class-AB amplifier at the bottom</td>
</tr>
<tr>
<td>30</td>
<td>V_{bn4}</td>
<td>Protected</td>
<td>Bias pin for NMOS to all the 4-stage class-AB amplifiers</td>
</tr>
<tr>
<td>31</td>
<td>V_{IN2,3-}</td>
<td>Protected</td>
<td>Input to the negative terminal of 3-stage class-AB amplifier at the bottom</td>
</tr>
<tr>
<td>32</td>
<td>V_{OUT7}</td>
<td>Protected</td>
<td>Output of 3-stage class-AB amplifier at the bottom</td>
</tr>
<tr>
<td>33</td>
<td>V_{bn3}</td>
<td>Protected</td>
<td>Bias pin for NMOS to all the 3-stage class-AB amplifiers</td>
</tr>
<tr>
<td>34</td>
<td>V_{OUT5}</td>
<td>Protected</td>
<td>Output of 3-stage pseudo class-AB amplifier at the bottom</td>
</tr>
<tr>
<td>35</td>
<td>V_{IN2,1-}</td>
<td>Protected</td>
<td>Input to the negative terminal of 3-stage pseudo class-AB amplifier at the bottom</td>
</tr>
<tr>
<td>36</td>
<td>Global V_{SS}</td>
<td>-ve</td>
<td>-</td>
</tr>
<tr>
<td>37</td>
<td>V_{DD2}</td>
<td>Protected</td>
<td>Vdd supply to all the four amplifiers that are at the bottom</td>
</tr>
<tr>
<td>38</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>39</td>
<td>V_{OUT9}</td>
<td>Protected</td>
<td>Output of 3-stage pseudo class-AB amplifier which is connected as voltage follower</td>
</tr>
<tr>
<td>40</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>
• Three-Stage I-I-N Pseudo-Class AB Amplifier with $C_{CB}$

The bias current is 10µA, the supply voltage $V_{DD}$ is 1.25V and $V_{bn2}$ is -322.6mV. Therefore the bias resistor is given by

$$R = \frac{V_{DD} - V_{bn2}}{I_{Bias}} = 157.3k\Omega$$ \hspace{1cm} (3)

Since it is supplying current to three amplifiers, the resistance should be three times less than the calculated.

$$R = 53k\Omega \text{ [Since three amplifiers]}$$ \hspace{1cm} (4)

Connect $V_{bn2}$ (pin18) to one end of the bias resistor and other end of resistor is connected to $V_{DD}$ (Pin16)

• Three-Stage I-N-I Pseudo-Class AB Amplifier

The bias current is 10µA, the supply voltage $V_{DD}$ is 1.25V, $V_{bp3}$ is 203.6mV and $V_{bn3}$ is -380.0mV. Therefore the bias resistor is given by

$$R = \frac{V_{bp3} - V_{bn3}}{I_{Bias}} = 58.3k\Omega$$ \hspace{1cm} (5)

Since it is supplying current to three amplifiers, the resistance should be three times less than the calculated.

$$R = 20k\Omega \text{ [Since three amplifiers]}$$ \hspace{1cm} (6)
Connect $V_{bp3}$ (pin10) to one end of the bias resistor and other end of resistor is connected to $V_{bn3}$ (Pin33)

- **Three-Stage Proposed Class AB Amplifier**

  The bias current is $10\mu A$, the supply voltage $V_{DD}$ is 1.25V and $V_{bn4}$ is -380mV. Therefore the bias resistor is given by

  \[ R = \frac{V_{DD} - V_{bn4}}{I_{Bias}} = 163k\Omega \]  

  (7)

  Since it is supplying current to three amplifiers, the resistance should be three times less than the calculated.

  \[ R = 53.5k\Omega \]  

  (Sincethreeamplifiers)  

  (8)

  Connect $V_{bn4}$ (pin30) to one end of the bias resistor and other end of resistor is connected to $V_{DD}$ (Pin16)

**Transient Measurement**

1. The amplifiers must be connected in inverting configuration as shown in Fig. [A.1]

2. Two 200k$\Omega$ resistors are used to achieve unity gain feedback

3. For three-stage I-I-N pseudo-class AB amplifier, a 200k$\Omega$ resistor is connected in between $V_{OUT1}$ (pin7) and $V_{IN-}$ (pin6) and another resistor to $V_{IN-}$ (pin6) and the input from function generator
Figure A.1: Test bench for measuring transient response of the amplifier.

4. Similarly, for three-stage I-I-N pseudo-class AB amplifier with $C_{CB}$, a 200kΩ resistor is connected in between $V_{OUT2}$ (pin14) and $V_{IN-}$ (pin15) and another resistor to $V_{IN-}$ (pin15) and the input from function generator.

5. For three-stage I-N-I pseudo-class AB amplifier, a 200kΩ resistor is connected in between $V_{OUT3}$ (pin9) and $V_{IN-}$ (pin11) and another resistor to $V_{IN-}$ (pin11) and the input from function generator.

6. For proposed three-stage class AB amplifier, a 200kΩ resistor is connected in between $V_{OUT4}$ (pin12) and $V_{IN-}$ (pin13) and another resistor to $V_{IN-}$ (pin13) and the input from function generator.

7. The positive terminal of all those amplifiers is shorted to $V_{IN1+}$ (Pin5) and it should be connected to ground of the function generator.

8. A rail-to-tail pulse signal of frequency 100kHz from a function generator is given to the 200kΩ resistor connected to negative terminal of the amplifiers.
9. Output terminal $V_{OUT1}$ (pin7), $V_{OUT2}$ (pin14), $V_{OUT3}$ (pin9), and $V_{OUT4}$ (pin12) of each amplifier is connected to load resistor and load capacitor in parallel to ground separately.

10. The outputs of each amplifier are observed on the scope and store it to the system

11. Tabulate the results of Slew Rate (SR) and Settling Time (ST).

**Power-Supply Rejection Ratio (PSRR)**

![Test bench for measuring PSRR of the amplifier.](image)

Figure A.2: Test bench for measuring PSRR of the amplifier.

1. For PSRR, the amplifiers must be closed-loop configuration. Short output node and negative terminal of the amplifier to form a closed-loop as shown in Fig. [A.3](image)
2. The positive terminal of all those amplifiers is shorted to $V_{IN1+}$ (Pin5) and it should be connected to ground of the function generator.

3. For three-stage I-I-N pseudo-class AB amplifier, short $V_{OUT1}$ (pin7) and $V_{IN-}$ (pin6).

4. Similarly, for three-stage I-I-N pseudo-class AB amplifier with $C_{CB}$, short $V_{OUT2}$ (pin14) and $V_{IN-}$ (pin15).

5. A 100mV amplitude sinusoidal signal from a function generator is in series with the DC voltage source and connect it to $V_{DD1}$ (pin4) as shown in Fig. A.3.

6. Output terminal $V_{OUT1}$ (pin7) and $V_{OUT2}$ (pin14) of amplifiers are connected to nominal load resistor (10kΩ) and load capacitor (100pF) in parallel to ground separately.

7. Find the RMS of input voltage in digital spectrum analyser

8. Find the RMS of output voltages of both the amplifiers in digital spectrum analyser

9. Subtract the input RMS from the output RMS to measure PSRR

10. Tabulate the results by varying the frequency of the sinusoidal signal

**DC Currents**

1. For DC currents, all the amplifiers in the top must be in inverting configuration. Use two 200kΩ resistor to achieve unity gain as shown in Fig. A.1

2. The positive terminal of all those amplifiers is shorted to $V_{IN1+}$ (Pin5) and it should be connected to ground.
Figure A.3: Test bench for measuring DC Currents of the amplifiers.

3. Connected digital multimeter (DMM) in series with the DC voltage source and connect it to $V_{DD1}$ (pin4) to measure the current.

4. One end of the 200kΩ resistor going to negative terminal of the amplifier $V_{IN-}$ is connected to a DC voltage source.

5. Give 0V, 1.25V and -1.25V to the input and measure the current through $V_{DD}$ which gives the total bias current of all the amplifiers. Divide by 4 to measure the total bias current to each amplifier.

6. Attach a resistive load of 1kΩ to one amplifier and measure the current and voltage for 1.25V and -1.25V of DC input. Subtract the total bias current measured in previous step from the measured current in this step to find the quiescent current of that particular amplifier.

7. Shift the load to the other amplifiers one by one and measure the DC quiescent current of each amplifier for particular load current.

8. Measure the output voltage using DMM to find the output sinking or sourcing current of the amplifier by dividing the voltage with 1kΩ resistance.

9. Tabulate the results to differentiate the class AB and pseudo-class AB amplifiers.
APPENDIX B

Maple
\[ \begin{align*}
\text{gain} &= Vout/Vin \\
wp1 &= \frac{\text{gm}1 \cdot (Vout - V2) \cdot s \cdot \text{Cc}}{\text{Rout}} + \text{Vx} = \frac{V1}{\text{R1}}, \quad i1 = \frac{(Vx - V2) \cdot s \cdot \text{Cc}}{1 + \text{s} \cdot \text{Cc} \cdot \text{Rc}}, \quad i1 = \frac{\text{Vout} + \text{Vx} \cdot \text{gm}1}{\text{Rout}} \cdot (i1, \text{V1}, \text{V2}, \text{Vx}, \text{Vout}) \bigg\} \quad s
\end{align*} \]
REFERENCES
REFERENCES


