Abstract—A heterodyne interferometric CMOS 8x8 phase sensor array was developed to measure the spatial phase distribution of an optical wavefront. This sensor is suitable for measuring rapidly changing surface profiles and characterizing fast turbulence. Using an acousto-optic modulation frequency of 80 MHz and beat frequency of 10 kHz, the system calculates 8-bit phase data at each location in the array at a rate equal to the beat frequency. The phase computation is performed locally, digitized, and stored in 8-bit SRAM. Implemented in a 0.5-µm 2P3M CMOS process, the measured RMS phase error is 1.49° (1 LSB) and mismatch has $\sigma = 4.76°$ (3.4 LSB). Experimental results, in agreement with theory, validate the proposed approach.

Index Terms—CMOS Integrated optics, Heterodyne optical phase sensor, Phase detector, Zero crossing, Gray-to-binary conversion, heterodyne interferometer.

I. INTRODUCTION

APPLICATIONS such as optical surface profiling, non-destructive testing, and adaptive optical correction require measurements of the spatial phase distribution associated with an optical wavefront. In the case of profiling, the characteristics of a surface can be observed as deviations in the phase of a reflected optical wavefront [1]–[3]. An accurate measurement of the phase variations across the wavefront gives a measure of the surface structure. In the case of adaptive optical correction, the optical wavefront phase from the subject of interest is measured with a wavefront sensor and, based on a measured or derived reference phase, corrections for aberrations are made with an adaptive mirror or similar device [4]–[6].

Optical phase measurement takes many forms. Our interest is with interferometric approaches. Non-heterodyning interferometric methods, in general, work by transforming the (directly non-measureable) phase into amplitude (intensity) by interfering the test wave (beam) of interest with a reference beam. A form of this approach known as phase shifting interferometry is used extensively in optical surface measurements [1], [2]. Heterodyning refers to the process of mixing the test wave with a reference wave of slightly different optical frequency. This mixing produces a low frequency intensity signal that carries the test wave optical phase. This signal can be measured and processed by conventional photo-detectors and electronic circuitry. A common aspect of all these techniques is that, after intensity measurements are made, a set of calculations must be performed to recover the optical phase values. The calculations are typically straightforward but for a pixilated sensor the time required to read out the sensor array and perform the calculations can be prohibitive for some fast-acting phenomena. Examples of such situations are surface measurements of rapidly changing surfaces or targets or optical path variations (turbulence) measurements associated with a fast-moving platform.

Several high-speed, optical phase sensing methods and devices have been described recently in the literature. References [7] and [8] demonstrate single photo-detector CMOS phase sensors. Advances in high-speed phase array imaging include a two-camera phased system approach [9], which utilizes separate CCD cameras with a 100 frame/s rate for sampling the interferometric pattern. An image sensor using a CMOS 6-T passive pixel array of 100 x 100 elements has been developed that uses a three-phase correlation method for phase determination and has been tested with heterodyne frequencies of up to 5.4kHz [10]. Our work also involves the development of a high-speed integrated heterodyne array phase sensing chip. In contrast to other heterodyne array sensors, our chip-based device employs a novel phase sensing scheme based on a fast parallel Gray-to-binary converter. This architecture allows operation at high heterodyne frequencies and the 8 x 8 element device described here is demonstrated.
with a heterodyne frequency of 10kHz. Our method provides phase measurements for each cycle of the heterodyne signal. This type of device allows high-speed optical phase imaging, that is, fast temporal measurement of the beating heterodyne signal at each location in a sensor array and allows a spatial phase map of an incident signal wavefront to be computed without scanning an image sensor. The promise of this approach is high-speed measurements with applications that include fast turbulence characterization and heterodyne array imaging, a technique capable of resolving target surface features, shape and position [11], [12]. The work we describe is an approach that incorporates array phase sensing circuitry directly on a CMOS sensor array.

II. HETERODYNE INTERFEROMETER

Fig. 1 shows an example heterodyne interferometer. Laser light is split into reference (P) and test (Q) paths and acousto-optic modulators (AOMs) shift the mean optical frequencies of each beam. The shifts are directly proportional to RF drive signal frequencies applied to the AOMs. For the P beam, the frequency shift is equal to $f_{\text{beat}}$ (typically about 80 MHz), whereas the frequency shift for the Q beam is higher by the amount $f_{\text{beat}}$ (typically 10 kHz). The beams are expanded. A splitter allows a portion of the test beam to interrogate a target surface, or perhaps an inhomogeneous medium before returning to the system. Using a beam splitter, the P and Q beams are recombined. The resulting optical intensity pattern contains a temporally beating signal at frequency $f_{\text{beat}}$. This signal effectively encodes the optical wavefront phase between the P and Q beams. For example, at a detector we might measure

$$I = I_1 + I_2 + 2\sqrt{I_1 I_2} \cos[2\pi f_{\text{beat}} t + (\phi_2 - \phi_1)],$$

(1)

where $I_1$ is the P beam intensity, $I_2$ is the Q beam intensity and $(\phi_2 - \phi_1)$ is the difference in the optical phase between the P and Q fields.

A. Zero Crossing Method

The proposed integrated array phase sensor uses a zero crossing technique to measure the phase at each location in the array. The zero crossing method is illustrated using Fig. 2. Signals at two locations in the array cross through zero, from positive to negative, at times $t_1$ and $t_2$. The relative phase $\Delta \phi$ between the two locations is calculated by

$$\Delta \phi = \frac{2\pi \Delta t}{T} = 2\pi f_{\text{beat}} (t_2 - t_1),$$

(2)

where $T$ is the time period of the beat frequency.

Random perturbations of zero crossings cause phase noise, which can be reduced by averaging over multiple cycles [13].

Phase sensors reported in [7] and [8] use the correlation and XOR phase-detection method, respectively. These techniques require lowpass filters to average the phase for multiple periods. The advantage is reduced noise, but the penalty is greatly increased response time (on the order of 307). On the other hand, the method of zero crossings allows for real-time changes in phase to be measured within one-to-two cycles.

III. DESIGN AND ARCHITECTURE

The proposed integrated phase sensor IC takes as input an optical wavefront with possibly time-varying phase variations and outputs K-bit digitized measurements of the relative phase at each of N x M equally-spaced locations.

Fig. 3 shows the architecture of the proposed optical phase sensor IC. It consists of an $N \times M$ array of phase detectors, row and column decoders, row drivers, a column multiplexer, a K-bit Gray counter, and a K-bit Gray-to-binary converter. The row and column select lines enable a single phase detector in the array to output the K-bit data stored in that phase detector.

A. Phase Detector Circuitry

The block diagram of a single phase detector is shown in Fig. 4. Each phase detector consists of a photo-diode with load, a tunable highpass (HP) filter, a comparator with programmable hysteresis, and K negative-edge triggered D flip-flops with output enable.

1) Photo-diode and highpass filter: Fig. 5(a) shows the conceptual schematic of the photo-diode and HP filter. The n+/p- photo-diode generates photo current in the order of nA, proportional to the intensity of the heterodyne light signal of frequency $f_{\text{beat}}$. This current is converted into the voltage $v_{PH}$ by two diode-connected PMOS transistors, $M_1$ and $M_2$. 

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operating in subthreshold, as shown in Fig. 5(b). The small-signal resistance of two series diode-connected transistors is \(2/g_m\), effectively doubling the small-signal amplitude of \(v_{PH}\).

The proposed optical phase sensor IC architecture is shown in Fig. 3. It consists of a tunable high-pass filter, a comparator, a counter, and a logic block. The filter is used to remove the dc offset and set the dc value to \(v_S\). The comparator, which operates in the subthreshold regime, is shown in Fig. 4. The output of the comparator is used to trigger the D flip-flops, which are used to count the number of transitions in the output during a single zero-crossing.

Adding hysteresis eliminates the possibility of multiple transitions in the output during a single zero-crossing.

3) Negative Edge-Triggered D Flip-Flops: Referring to Fig. 4, at every negative-edge of the square wave \(v_{COMP}\), the \(K\)-bit Gray code counter values are stored in \(K\) D flip-flops. The outputs of the flip-flops are enabled when \(Row[n]\) is high. The proposed implementation of \(K\) negative edge-triggered D flip-flops with output enable, shown in Fig. 7, reduces transistor count by approximately a factor of two compared to a conventional master-slave D flip-flops. This implementation uses negative edge detection logic, \(K\) SRAM cells and \(K\) tri-state inverters. The signal \(v_{PULSE}\) goes high for a short duration in response to the negative-edge of the signal \(v_{COMP}\). While \(v_{PULSE}\) is high, the \(K\) SRAM cells store the \(K\) Gray code counter bits corresponding to the exact negative-going zero crossing time of the incident light at location \((n,m)\). When signal \(Row[n]\) goes high, the phase detector outputs the stored phase data onto the \(K\)-bit column bus \(Gray_{out}[n, m]\).

A tunable HP filter is used to remove the dc offset and set the dc value to \(v_S\). In Fig. 5(b), \(M_3\) operates in the subthreshold ohmic region where it behaves as a variable large-value resistor. The filter has a corner frequency that is tunable with bias current \(I_{Gm}\), given by

\[ f_c = \frac{g_m}{2\pi C}, \]

where \(g_m = kI_{Gm}/V_T\), \(V_T\) is the thermal voltage, and \(k\) is the gate coefficient, in the range 0.6–0.9. The HP filter corner frequency \(f_c\) is set to be much less than \(f_{heat}\).

2) Comparator with hysteresis: Using the comparator shown in Fig. 6, the sinusoidal signal \(v_{HP}\) in Fig. 4 is converted into a square wave \(v_{COMP}\). Programmable hysteresis current \(I_{Hyst}\) (where \(I_{Hyst} < I_{Bias}\)) effectively imbalances the input differential pair using positive feedback [14], [15]. Adding hysteresis eliminates the possibility of multiple transitions in the output during a single zero-crossing.

4) Phase Detector Simulations: Simulations of a single phase detector block are shown in Fig. 8. We assume moderate interference between the reference and test waves, such that visibility is 0.5. Moreover, the RF-modulated beams are assumed to have low optical power, on the order of nW, yielding photo-currents below 1nA. The corresponding photo-diode current \(i_{PH}\) has a dc offset of 0.1nA and amplitude of 0.05nA, as shown in Fig. 8(a).

The photo-diode current \(i_{PH}\) is converted to a sinusoidal voltage \(v_{PH}\) with a dc offset that is light-level dependent, as shown in Fig. 8(b). The dc offset of \(v_{PH}\) is removed and set to \(V_S = -1.25V\) by the HP filter. The signal \(v_{HP}\), Fig. 8(c), is digitized to become \(v_{COMP}\). Fig. 8(d). Fig. 8(e), \(v_{PULSE}\), is created using the negative edge-detection logic.

B. Gray Counter

Analog-to-digital encoding of the phase is accomplished using a \(K\)-bit counter operating at a frequency \(f_{CLK} = 2^K f_{heat}\). One LSB (least-significant bit) of the counting A-to-D converter, in terms of phase, corresponds to 360° / \(2^K\). For \(K = 8\) and \(f_{heat} = 10kHz\), the counter frequency is \(f_{CLK} = 2.56\).
MHz and the resolution of the digitized phase is 1 LSB = 1.41°.

The signal \( v_{PULSE} \) in Fig. 8(e), which results from an optical signal with unknown phase, is asynchronous with respect to the counter clock. If a binary counter is sampled asynchronously, large errors can result [16]. As such, a Gray counter is used, reducing the maximum possible error to less than 1 LSB.

\[ \frac{1}{2^{n}} \leq \frac{1}{2^{8}} = 0.00390625 \leq 1 \text{ LSB} \]

Since 8-bit Gray codes have a minimum of 100% carry, the maximum possible error is 1 LSB.

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optical signals is varied such that different number of bits are varying in the outputs for different phase values. Fig. 11 shows the best-fit model using linear regression (LR) on the measured relative phase between PDs (5,5) and (2,2) and between PDs (7,7) and (2,2). The offset is 14.5° and slope is 0.98. The RMS error of the measured values to the LR model is 1.46°, corresponding to 1.0 LSB.

D. Mismatch in Phase Detectors
The phase detectors in row 4 and the phase detectors along the diagonal of the 8 x 8 array were measured using a single LED at constant amplitude, frequency, and phase. The outputs of the phase detectors are plotted in Fig. 13. The average output value is 258°. The mismatch in phase detectors is calculated as σ = 4.76°, corresponding to 3.4 LSBs.

Performance characteristics of the proposed CMOS phase sensor IC are summarized in Table I.

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**Fig. 10.** Micrograph of the proposed integrated sensor system (active area: 1200μm × 1200μm).

**Fig. 11.** Test Setup displaying two LEDs used and their illumination of phase detectors centered at locations (2,2) and (7,7).

**Fig. 12.** Relative phase between optical signals of two detector locations.

**Fig. 13.** Measurements illustrating mismatch in phase detectors (σ = 4.76°).

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**TABLE I**

<table>
<thead>
<tr>
<th>CHARACTERISTICS OF PROPOSED CMOS PHASE SENSOR IC</th>
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**TABLE II**

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<td>Pixel Array</td>
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<td>Resolution</td>
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<td>$f_{\text{beat}}$</td>
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<td>Data Rate</td>
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V. SCALABILITY OF PHASE SENSOR

In Table II, we predict the scalability of the proposed CMOS Phase Sensor based on increased die size and scaled process dimensions. The current design, implemented in the AMI 0.5-µm process on a 1.5mm x 1.5mm die, permitted a maximum array size $N \times M$ equal to 8 x 8. The data rate, computed using,

$$\text{Data Rate} = f_{\text{beat}} \times N \times M \times \text{Resolution}, \quad (5)$$

is 0.64 MB/s for the current work.

For a larger die size of 5 mm x 5 mm in the same process, the predicted pixel array size is 40 x 40 with a corresponding increase in data rate to 16 MB/s. Such a high data throughput may require high-speed sensing schemes, similar to those found in SRAM arrays [18]. Scaling to a design process with a smaller feature size, such as the TSMC 0.18-mm process, results in reduced pixel size and increased pixel array size. The predicted data rate is 100 MB/s. For both of these larger array sizes, the issue of a “rolling shutter” is imposed. Essentially, this means that the data collected from the first row in the array would be acquired and read out almost one period ($1/f_{\text{beat}}$) prior to that of the last row in the array.

VI. CONCLUSIONS

We developed a new CMOS sensor array for fast and accurate measurement of the spatial phase distribution associated with an optical wavefront for use in heterodyne interferometry. The proposed sensor finds applications in optical surface profiling, non-destructive testing and 3D imaging. The sensor is amenable to 3D Systems-on-Chip integration wherein the photo-detector, low-power analog circuitry, and digital circuitry could all be stacked, in an effort to simultaneously decrease area and increase fill factor.

REFERENCES


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