Low Dropout (LDO) Voltage Regulator Design Using Split-Length Compensation

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Abstract—We explore the application of split-length compensation to the design of a three-stage low dropout (LDO) voltage regulator. Initially, we review three basic compensation techniques, Miller, cascode, and split-length, and demonstrate their use in a multi-stage amplifier. It is found that stable designs are possible using single Miller compensation, whereas both cascode and split-length compensation require a Miller compensation network in parallel. Finally, we compare the three compensation techniques in terms of quiescent current, area, dropout voltage, unity-gain frequency, line and load transient response, and power supply rejection. For the LDO architecture selected, it is found that cascode and split-length compensation offer very similar performance, with the exception of quiescent current and area. Cascode compensation required 24% less total compensation capacitance, whereas split-length compensation used 14% less quiescent current.

Index Terms—Split-length compensation, Miller, cascode, single Miller compensation (SMC), Multi-stage amplifiers, Low Dropout (LDO) voltage regulators.

I. INTRODUCTION

As supply voltages scale down with advanced process nodes, low voltage, high-gain amplifiers are realized by cascading multiple gain stages. However, each gain stage inevitably introduces low-frequency poles which tend to degrade stability. The choice of compensation network impacts a wide range of amplifier performance measures, including power consumption, silicon area, unity-gain frequency and power-supply rejection. Two widely understood and adopted compensation techniques are Miller [1]-[3] and cascode compensation [4]-[20].

Saxena and Baker recently introduced a third compensation technique, split-length compensation [21]-[22]. More recently, it was called “pseudo-cascode” by the authors in [22]. Split-length compensation is particularly suited to low-voltage amplifiers, as the headroom requirement is almost half that of cascode compensation. In [24], the application of split-length compensation to the design of a wide-range of high-performance amplifiers, including LDOs, is described.

The goal of this work is to quantify the benefits of applying split-length compensation to the design of LDOs, comparing split-length to the better-known Miller and cascode techniques. LDOs are particularly important in today’s portable electronic devices, which require clean power at minimal cost [12]-[15].

This paper is organized as follows: The application of Miller, cascode, and split-length compensation methods is described in Section II. Section III discusses the implementation of the three-stage LDO. In Section IV, the three methods are compared through a wide range of simulation experiments. Discussion and conclusions follow.

II. COMPENSATION TECHNIQUES

Fig. 1 depicts the architecture of a generic three-stage LDO. Let the transconductance, equivalent resistance to ground and lumped parasitic capacitance of the $i$th stage be represented by $G_{mi}$, $R_i$ and $C_i$ respectively. At the output of the third stage, $R_{OUT}$ is the parallel combination of $R_3$ and $R_L$, the external load resistance. Similarly, $C_{OUT}$ is the sum of $C_3$ and $C_L$, the load capacitance. Parasitic capacitance $C_{GD}$ is due to the large pass transistor of the output stage.

![Fig. 1. LDO architecture employing single Miller compensation.](image)

The low-frequency gain of the amplifier $A_{DC}$ is the product of the gain of all three stages:

$$ A_{DC} = G_{m1}R_1G_{m2}R_2G_{m3}R_{OUT}. $$

Small-signal quantities $G_{m3}$ and $R_{OUT}$ are functions of load current $I_L$ which, in a typical LDO design, may vary by several orders of magnitude. $R_{OUT}$ is inversely proportional to $I_L$ whereas $G_{m3}$ increases with $I_L$ at a rate that is sub-linear.
As such, \( A_{DC} \) tends to fall off at high load currents. The challenge of stabilizing an LDO is enhanced by these expected variations in \( R_{OUT} \), \( g_{mC} \), and \( A_{DC} \). Very often, a large external load capacitance is required.

### A. Single Miller Compensation

While more complex Miller compensation techniques are possible, the architecture of Fig. 1 employs single Miller compensation (SMC) [14], [16]. Compensation resistor \( R_M \) is placed directly between the output of the third stage \( V_{OUT} \) and the output of the first stage \( V_1 \).

Assuming \( C_{OUT} \gg C_M, C_2, C_GD, \) and \( C_M, C_2, C_GD \gg C_1 \), and that the poles are widely separated, circuit analysis of the architecture in Fig. 1 yields the following equations for the dominant poles and zero:

\[
\begin{align*}
\omega_p1 &= \frac{1}{R_{OUT} C_{OUT} + R_M C_M g_m n_2 R_2 g_m n_3 R_{OUT}} \\
\omega_p2 &= \frac{C_{OUT} + R_M C_M g_m n_2 R_2 g_m n_3}{C_{OUT} C_M (R_1 + R_M)} \\
\omega_z1 &= \frac{1}{R_M C_M}
\end{align*}
\]  

For very large \( C_{OUT} \), the first pole \( \omega_p1 \approx 1/C_{OUT} R_{OUT} \). Due to the variation in \( R_{OUT} \) with load current, this output pole moves towards high frequencies at high load currents. The second dominant pole occurs at node \( V_1 \), the output of the first stage. For \( C_{OUT} \) very large, \( \omega_p2 \approx 1/C_M (R_1 + R_M) \). The left-half plane zero \( \omega_z1 \) helps guarantee stability over a wide range of output current.

### B. Cascode Compensation

In Fig. 2, cascode compensation is employed between nodes \( V_{OUT} \) and \( V_1 \) with the addition of capacitor \( C_C \) in series with current buffer \( g_{mC} \). Stability could not be achieved over a wide range of load currents without the inclusion of the parallel Miller compensation network, as shown.

Under the assumptions described earlier, circuit analysis of Fig. 2 yields the following equations for the dominant poles and zero:

\[
\begin{align*}
\omega_p1 &= \frac{1}{R_{OUT} C_{OUT} + R_M (C_C + C_M) g_m n_2 R_2 g_m n_3 R_{OUT}} \\
\omega_p2 &= \frac{C_{OUT} + R_M (C_C + C_M) g_m n_2 R_2 g_m n_3}{C_{OUT} C_M (R_1 + R_M) + R_M C_M R_2 C_C R_M g_m n_2 g_m n_3} \\
\omega_z1 &= \frac{1}{R_M C_M}
\end{align*}
\]  

As for Miller compensation, the first pole occurs at the output node and the second at node \( V_1 \). The zero due to the Miller compensation is absolutely vital for stability over a wide range of output currents.

### C. Split-Length Compensation

The technique of split-length compensation was introduced in [19]. It is accomplished by splitting the length \( L \) of a single transistor into two shorter lengths, \( L_1 \) and \( L_2 \). Splitting of an NMOS device is depicted in Fig. 3, in which \( L_1 + L_2 = L \).

\[
\omega_p1 = \frac{1}{R_{OUT} C_{OUT} + R_M g_{mC} R_2} \\
\omega_p2 = \frac{C_{OUT} + R_M g_{mC} g_m n_2}{C_{OUT} C_M (R_1 + R_M) + R_M C_M R_2 g_m n_3} \\
\omega_z1 = \frac{1}{R_M C_M}
\]  

The form of the pole-zero equations are identical to those of cascode compensation. The only difference is that roughly half of the current through transistor \( C_C \) is actually fed back through current buffer \( g_{mC2} \), assuming \( g_{mC1} = g_{mC2} \). As such, the “effective” cascode compensation capacitance is reduced to 0.5\( C_C \) in (3) when applied to split-length compensation.

### III. THREE-STAGE LDO IMPLEMENTATION

The schematic of a three-stage LDO employing single Miller compensation is shown in Fig. 5. The feedback path is indicated with a dashed line from node \( V_{fb} \) to \( V_{fb}' \). The first stage is an NMOS differential amplifier. The differential input \( (V_{fb'} - V_{fb}) \) corresponds to \( V_{IN} \) in the small-signal models of Figs. 1, 2, and 4. The second stage is a PMOS non-inverting common-source amplifier. The output stage is a common-source amplifier realized with the huge pass.
transistor $M_{PAS}$. The second stage employs an adaptive biasing technique described in [14]-[15].

Only the differential amplifier changes while incorporating the two other types of compensation. Fig. 6 shows the necessary changes to the differential amplifier to incorporate cascode and split-length compensation into the LDO.

The baseline Miller-compensated LDO was designed in a 0.5-$\mu$m 2P3M process under the following constraints: a load current range from 100 $\mu$A to 100 mA, a 1.2-V reference voltage, a 1.5-V output voltage, an external load capacitance of 1 $\mu$F, a quiescent current of 21 $\mu$A at minimum load current and 75 $\mu$A at maximum load current, a low-frequency gain of 63 dB at maximum current load, a dropout voltage of 106 mV, and a minimum phase margin of 45°. These constraints help serve as controls for the simulation experiments described in the next section.

IV. SIMULATION EXPERIMENTS

A series of simulation experiments were conducted to measure the performance of the three compensation techniques: Miller, cascode (with parallel Miller) and split-length (with parallel Miller). Fig. 7 shows the simulated phase margin as a function of load current $I_{LOAD}$. It is apparent that the minimum phase margin is 45° for all three designs.

Fig. 8 shows the output voltage $V_{OUT}$ in response to a 1-V change in the input voltage $V_{LINE}$. Input rise and fall times are 100 ns each. The large variation in output voltage for Miller compensation is reduced by a factor of 5 for cascode and split-length. Fig. 9 shows the output response to a change in load current $I_{LOAD}$ from minimum to maximum values with rise and fall times of 200 ns and 500 ns, respectively. In this case, the reduction of output voltage variation for the cascode and split-length designs is not quite a factor of 2.

Fig. 10 shows the simulated power supply rejection, measured at a load current of 1 mA. Power supply rejection is measured with the LDO in a closed-loop configuration by injecting a sinusoidal source in series with the line voltage. Over the frequency range of 400 Hz to 50 kHz, cascode and split-length cascode compensation improves PSRR by 13 dB.

![Fig. 5. Schematic of three-stage LDO using single Miller compensation.](image)

![Fig. 6. Schematic of first-stage differential amplifier allowing for (a) cascode compensation through node $V_f$ and (b) split-length compensation through node $V_x$.](image)

![Fig. 7. Phase margin as a function of load current for (a) Miller, (b) cascode, and (c) split-length compensation schemes.](image)

![Fig. 8. Line transient response for (a) Miller, (b) cascode, and (c) split-length compensation schemes. An offset was added for visibility.](image)

![Fig. 9. Load transient response for (a) Miller, (b) cascode, and (c) split-length compensation schemes. An offset was added for visibility.](image)
split-length compensation schemes.

Fig. 10. Power supply rejection as a function of frequency for (a) Miller, (b) cascode, and (c) split-length compensation schemes.

V. DISCUSSION AND CONCLUSIONS

Table I summarizes the performance characteristics of the three LDO designs. For virtually all of the performance measures summarized in Table I, cascode compensation and split-length compensation, in parallel with Miller compensation, outperform Miller compensation alone. On the other hand, cascode and split-length compensation have very similar simulated performance, except for total compensation capacitance and quiescent current at minimum load current. The tradeoff, therefore, appears to be mostly between area and power.

In a direct comparison of the split-length and cascode compensation schemes, split-length shows a reduction in quiescent current of 14% at minimum load, whereas cascode shows a reduction in total compensation capacitance of 24%. However, the area of this LDO design is dominated by the huge pass transistor, sized 30 mm x 0.6 μm, which occupies a silicon area corresponding to a 60 pF poly1-poly2 capacitor. As such, a 24% reduction in compensation capacitance results in roughly a 6% decrease in total area.

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>LDO Compensation Network</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total Compensation Capacitance</td>
<td>47.0 pF</td>
</tr>
<tr>
<td></td>
<td>15.1 pF</td>
</tr>
<tr>
<td></td>
<td>19.9 pF</td>
</tr>
<tr>
<td>Qiescent Current @ I_L = 100 μA</td>
<td>21.9 μA</td>
</tr>
<tr>
<td></td>
<td>25.7 μA</td>
</tr>
<tr>
<td></td>
<td>22.0 μA</td>
</tr>
<tr>
<td>Qiescent Current @ I_L = 10 mA</td>
<td>75.0 μA</td>
</tr>
<tr>
<td></td>
<td>78.8 μA</td>
</tr>
<tr>
<td></td>
<td>75.1 μA</td>
</tr>
<tr>
<td>Unity-Gain Frequency @ I_L = 100 μA</td>
<td>35.9 kHz</td>
</tr>
<tr>
<td></td>
<td>75.8 kHz</td>
</tr>
<tr>
<td></td>
<td>76.8 kHz</td>
</tr>
<tr>
<td>Unity-Gain Frequency @ I_L = 100 mA</td>
<td>1.23 MHz</td>
</tr>
<tr>
<td></td>
<td>1.86 MHz</td>
</tr>
<tr>
<td></td>
<td>1.74 MHz</td>
</tr>
<tr>
<td>Line Transient Repose ΔV_OUT</td>
<td>232 mV</td>
</tr>
<tr>
<td></td>
<td>42.5 mV</td>
</tr>
<tr>
<td></td>
<td>46.1 mV</td>
</tr>
<tr>
<td>Load Transient Repose ΔV_OUT</td>
<td>44.2 mV</td>
</tr>
<tr>
<td></td>
<td>25.1 mV</td>
</tr>
<tr>
<td></td>
<td>24.2 mV</td>
</tr>
<tr>
<td>PSR @ I_L = 1mA and f = 1 kHz</td>
<td>47.0 dB</td>
</tr>
<tr>
<td></td>
<td>61.6 dB</td>
</tr>
<tr>
<td></td>
<td>60.9 dB</td>
</tr>
<tr>
<td>PSR @ I_L = 1mA and f = 100 kHz</td>
<td>18.5 dB</td>
</tr>
<tr>
<td></td>
<td>30.9 dB</td>
</tr>
<tr>
<td></td>
<td>31.1 dB</td>
</tr>
</tbody>
</table>

REFERENCES