A 1.21V, 100mA, 0.1µF-10µF Output Capacitor Low Drop-Out Voltage Regulator for SoC Applications

Annajira Garimella and Paul M. Furth
Klipisch School of Electrical and Computer Engineering
New Mexico State University, Las Cruces, NM 88003 USA
{annaj, pfurth}@nmsu.edu

Abstract—A 1.21V output, 100mA, 0.1µF-10µF output capacitor, ESR-independent, low voltage, low drop-out voltage regulator for portable power applications is designed and fabricated in a 0.5µm CMOS process with an area of 0.22 mm². The use of a wide-range output capacitor LDO enables reduced target system PCB size and Bill of Materials (BOM). A 0.05%/V line regulation, 0.001%/mA load regulation with 220mV drop-out is measured. LDO-specific pole-zero and optimal stability analyses are detailed.

I. INTRODUCTION

Power management circuits are becoming ubiquitous and challenging, with the proliferation of System-on-Chip (SoC) integration and functionality. Traditionally the Power Management Unit (PMU), consisting of regulated power supply circuits, was implemented as a separate design or as an off-the-shelf IC. SoCs with an integrated PMU enable the design of electronic systems with drastically reduced PCB area, number of external components and BOM [1].

LDOs often require a large off-chip external output capacitor for stability and improved transient response, which cannot be integrated on the SoC. Capacitor-free, low value and wide-range output capacitor features are becoming predominantly important for LDOs [2]-[6]. The proposed LDO is unconditionally stable with 0.1µF–10µF ceramic or MLCC output capacitors. An additional feature of the LDO is a digital Power Good output. This LDO is aimed for battery-powered micro-processors and micro-controllers.

II. COMPENSATION NETWORK

The choice of frequency compensation is the key for the stability of the proposed wide-range output capacitor LDO.

In conventional Miller compensation, shown in Fig. 1, the compensation capacitor forms a feedforward path [7] that couples the input node of the second stage $V_f$ directly to the output terminal $V_{out}$, introducing a right-half-plane (RHP) zero. Circuit analysis of Fig. 1 gives the location of this RHP zero at

$$\omega_{z,miller} = s_{mp}/[C_{miller} - R_2 s_{mp} + s_{gd,pass}]. \quad (1)$$

This RHP zero can be eliminated by proper selection of $R_2$. However, elimination of this RHP zero will further introduce parasitic zeros one at LHP, one at RHP given by

$$\omega_{z,miller} = \pm s_{mp} / [R_2 C_{miller} C_{gd,pass}]. \quad (2)$$

Alternatively, cascode compensation also known as Ahuja compensation, introduced in [7]-[8] and utilized in [3]-[4], [9]-[12], uses Miller compensation with a common-gate transistor as a current buffer, obviating the RHP zero, introducing a left-half-plane (LHP) zero and thus improving the stability. As shown in Fig. 2, the compensation capacitor is connected between $V_{out}$ and the internal node $V_i$ through a common-gate transistor amplifier $M_{cg}$, eliminating the feedforward path. $I_c$ is a dc bias current entering and leaving node $V_i$, forming a virtual open at node $V_i$.

The two-stage op-amp in [11] utilizes cascode compensation and unconditional stability is achieved with an output capacitive load from 10pF (no-load) to 100nF. This kind of output capacitance variation is desirable in LDOs. Section III focuses on the design of wide-range output capacitor, ESR-independent LDO architecture.
III. DESIGN OF THE PROPOSED LDO

Fig. 3 shows the schematic of the proposed low drop-out voltage regulator, which consists of an error amplifier, a PMOS pass transistor \( M_{pass} \), a sampling network, a cascode compensation network with replica bias and bias transistors. \( M_{cg} \) is the common-gate transistor amplifier, or the cascode transistor, used for compensation. The compensation capacitor \( C_{cas} \) is connected between the output node \( V_{out} \) and the source terminal of transistor \( M_{cg} \).

The dc bias current sinking from \( V_j \) to ground through \( M_4 \) and \( M_6 \) is \( I_s \). A replica bias, similar to the one in [9], formed by \( M_{cg} \) and \( M_6 \) is utilized to source \( I_s \) at node \( V_j \). Current mirror transistors \( M_3 \) and \( M_4 \) are reutilized instead of using additional PMOS bias transistors. Transistor \( M_{cg} \) is also a cascode transistor, and reduces \( V_{DS} \) mismatch between \( M_6 \) and \( M_4 \) and improves current matching. Rather than using a separate voltage \( V_{cg} \) as in Fig. 2, the gate terminals of \( M_4 \) and \( M_{cg} \) are connected to the voltage reference \( V_{ref} \). The dc current \( I_s \) is a scaled version of \( I_{bias} \) to reduce the total quiescent current.

Small value capacitors \( C_{f1} \) and \( C_{f2} \) are connected in parallel with sampling feedback resistors \( R_{f1} \) and \( R_{f2} \), respectively, to filter high frequency noise and to improve high frequency response, as described in [5].

A. Pole-Zero Analysis

Small signal equivalent model of the LDO using cascode compensation is shown in Fig. 4. The loop-gain transfer function of the LDO is given by

\[
T(s) \equiv \frac{v_{ph}}{v_{in}}(s) = \frac{A_{DC}(1 + s\omega_{cas})(1 + s\omega_{par})}{(1 + s\omega_{p1})(1 + s\omega_{p2})(1 + s\omega_{p3})(1 + s\omega_{p4})} \quad (1)
\]

where \( A_{DC} \) is the DC loop gain. The system has three zeros and four poles. \( R_{f1} \) is the resistance, \( C_1 \) is the capacitance and \( g_{ms} \) is the transconductance associated with node \( V_j \). The transconductance of common-gate transistor amplifier \( M_{cg} \) is \( g_{mcg} \). \( R_j \) is the equivalent output resistance given by \( R_{pass}(R_{fj} + R_{f2}) \). \( C_{out} \) is the output capacitance. \( C_{td,pass} \) is the gate-drain capacitance and \( g_{mp} \) is the transconductance of the pass transistor \( M_{pass} \). Note that \( C_1 = C_{gd} + C_{p2} + C_{p3,pass} \).

\( C_{td,pass} \) and \( C_{cas} \) are of the same order and have typical values of 10–25pF. As such, \( C_{td,pass} \) cannot be ignored. Capacitors \( C_{f1} \) and \( C_{f2} \) are 1pF each and are neglected in the frequency analysis. The given pole-zero analysis for the LDO includes \( C_{td,pass} \) and the ESR of the output capacitor \( R_{esr} \).

The DC loop gain \( A_{DC} \) is

\[
A_{DC} = \beta g_{m1}s g_{mp} R_{f1} R_2 , \quad (2)
\]

where the feedback factor \( \beta \) is given by \( R_{f2}/(R_{fj} + R_{f2}) \). The dominant LHP zero due to cascode compensation is

\[
\omega_{cas} = - g_{mcg}/C_{cas} . \quad (3)
\]

This LHP zero helps to increase the bandwidth. The LHP zero due to the ESR of the output capacitor \( C_{out} \) is

\[
\omega_{esr} = -1/R_{esr} C_{out} . \quad (4)
\]

The RHP zero due to parasitic \( C_{gd,pass} \) is given by

\[
\omega_{par} = + g_{mp}/C_{gd,pass} . \quad (5)
\]

Assuming that the poles \( \omega_{p1,2,3} \) and \( \omega_{p3} \) are three distinct poles, their equations are given in Table I. \( \omega_{p4} \) is located at very high frequency and is neglected.

B. Optimum Phase Margin

Assuming that \( \omega_{p3} \) and \( \omega_{p4} \) are located much higher frequencies than the unity-gain frequency (UGF), the phase margin \( \varphi \) is given by [4],[11]

\[
\varphi = 90^\circ - \arctan \left( \frac{1}{S} \right) + \arctan \left( \frac{1}{L} \right) , \quad (6)
\]

where larger stability quality factor \( S \), corresponds to larger...
phase margin. $L$ corresponds to effect of LHP zero $\alpha_{\text{cas}}$ on the phase margin and larger the value of $L$, larger is the improvement in phase margin. $S$ is calculated as

$$ S = \alpha_{\text{ps}} \cdot \omega_{\text{UGF}} = \alpha_{\text{ps}} / A_{\text{DC}} \alpha_{\text{ps}} \cdot \omega_{\text{UGF}}. \tag{7} $$

$L$ is calculated as

$$ L = \alpha_{\text{UGF}} / \alpha_{\text{cas}}. \tag{8} $$

Ignoring the effect of $L$ on phase margin, the minimum phase margin will occur either at $\partial S / \partial g_{\text{mp}} = 0$ or at $\partial S / \partial C_{\text{out}} = 0$. Solving $\partial S / \partial g_{\text{mp}} = 0$ for optimum $g_{\text{mp}}$,

$$ g_{\text{mp}} = C_{\text{out}} / [R(C_{\text{out}} + C_{\text{gd, pass})}] \cdot \tag{9} $$

Substituting (9) into (7),

$$ S_{\text{min}} = \frac{4}{g_{\text{mp}} R_{1}} \frac{(C_{\text{out}} + C_{\text{gd, pass})}}{(C_{1} + C_{\text{gd, pass})}} \cdot \tag{10} $$

Solving $\partial S / \partial C_{\text{out}} = 0$ will also result in same $S_{\text{min}}$ as in (10). The value of the compensation capacitor $C_{\text{cas}}$ is given by

$$ C_{\text{cas}} = \frac{g_{\text{mp}} R_{1}(C_{1} + C_{\text{gd, pass})}}{4 \tan(90^\circ - \varphi)} - C_{\text{gd, pass}}. \tag{11} $$

Fig. 5 shows the simulation of the loop gain and phase response of the proposed LDO.

C. Power Good Output

A Power Good output $V_{\text{reg}}$ is an important feature available in the commercial LDOs [13]. It can be used to implement a power-on-reset or low-battery indicator in portable appliances and functions as a supply voltage supervisor for the output voltage. It is asserted digital low (high) when the output of the LDO falls below (above) its normal regulating level. The Power Good output is obtained by comparing the feedback voltage $V_{\text{fb}}$ with the power good reference voltage $V_{\text{PGood}}$. $V_{\text{PGood}}$ can be chosen as $x\%$ of the regulated output voltage $V_{\text{out}}$, so that the power-up sequence of the microprocessor will resume whenever $V_{\text{out}}$ exceeds $x\%$ of its nominal value.

IV. EXPERIMENTAL RESULTS

The proposed LDO has been implemented using a triple-metal double-poly 0.5µm CMOS process with nominal $V_{\text{DD}} = -0.95\text{V}$ and $V_{\text{TN}} = 0.73\text{V}$. Fig. 6 shows the micrograph of the LDO. An external voltage reference $V_{\text{ref}}$ of 1.1V was chosen. An on-chip compensation capacitor $C_{\text{cas}}$ of 25pF is used. The total experimental quiescent current $I_{\text{q}}$ (including power good circuitry) is 111µA with an $I_{\text{bias}} = 10\mu\text{A}$ and 8.3µA with an $I_{\text{bias}} = 250\mu\text{A}$.

Fig. 7 shows the measured power-up and power-down of the proposed LDO. Fig. 8 shows the measured line transient response of the proposed LDO for $C_{\text{out}} = 0.1\mu\text{F}-10\mu\text{F}$ for $V_{\text{in}}$ change from 1.5V to 2.5V. Fig. 9 shows the measured load transient response of the proposed LDO for 0.1µF–10µF output capacitor values when $I_{\text{load}}$ is varied from 1mA to 100mA. The proposed LDO provides excellent regulation and response to line and load transients with an output capacitor as small as 0.1µF with an ESR of as little as 0 Ohms. The performance of the proposed LDO is summarized in Table II. Table III provides comparison of different LDOs. The Figure of Merit of [3], given by (11), is used to compare different LDOs.

$$ FOM = \frac{C_{\text{out}} \Delta V_{\text{out}}}{I_{\text{load, max}} l_{\text{q}}} \tag{11} $$

The smaller the FOM, the better is the performance of the LDO. The proposed LDO has the smallest FOM, compared to other LDOs and has very high current efficiency of 99.89%.

V. CONCLUSIONS

This paper presents a wide-range output capacitor, ESR-independent, CMOS low-drop-out voltage regulator, which utilize cascode compensation with replica bias to improve stability. The simulation and experimental results demonstrate the effectiveness of the proposed approach.
A Low Noise, High PSRR Low
Output Regulator with Reverse Current Protection

Smooth

Load Regulation, Δ
Line Regulation, Δ

Max. Measured
Input voltage range,

Fig. 6. Micrograph of the proposed LDO (762µm x 284µm).

Fig. 7. Measured power-up and power-down of proposed LDO. Input Vₚₒₚ off, dropout and regulating region of Vₚₒₚ and Power Good output VₚＧ can be seen.

Fig. 8. Measured line transient response of the proposed LDO.

Fig. 9. Measured load transient response of the proposed LDO.

Table III. Performance Comparison of Previously Reported LDOS.

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Vₒₒ(V)</td>
<td>0.35µm twin-well CMOS</td>
<td>1.5µm CMOS</td>
<td>0.5µm CMOS</td>
<td>0.5µm CMOS</td>
</tr>
<tr>
<td>Iₒₒ(max) (mA)</td>
<td>1.8–3.15</td>
<td>3.0–4.5</td>
<td>3.3</td>
<td>1.21</td>
</tr>
<tr>
<td>Vₒₒ(max) (mV)</td>
<td>200mA</td>
<td>150mA</td>
<td>400mA</td>
<td>100mA</td>
</tr>
<tr>
<td>Vₒₒ(cap) (mV)</td>
<td>0.2</td>
<td>0.2</td>
<td>0.2</td>
<td>0.22</td>
</tr>
<tr>
<td>Output Capacitor range</td>
<td>1µF</td>
<td>0.3µF–2.7µF</td>
<td>1µF, ESR=10mΩ</td>
<td>0.1µF–10µF</td>
</tr>
<tr>
<td>Iₒₒ at Full load</td>
<td>320µA</td>
<td>-</td>
<td>100µA</td>
<td>8.3µA</td>
</tr>
<tr>
<td>ΔVₒₒ</td>
<td>65mV with 1µF Cap</td>
<td>15.8mV with 1µF Cap</td>
<td>6.5mV with 1µF Cap</td>
<td>120mV with 0.1µF Cap</td>
</tr>
<tr>
<td>FOM (ns)</td>
<td>0.027</td>
<td>-</td>
<td>0.0041</td>
<td>0.0099</td>
</tr>
<tr>
<td>Current efficiency at Iₒₒ(max)</td>
<td>99.8%</td>
<td>-</td>
<td>99.97%</td>
<td>99.99%</td>
</tr>
</tbody>
</table>

VI. ACKNOWLEDGMENTS

The authors thank MOSIS for fabrication, Sri Raga Sudha Garimella, Intel Corporation, Hillsboro, OR for her support with simulations and layout. Also sincere thanks to Sheetal Liddar and Stewie Kwan of Texas Instruments Inc., Dallas, TX for their insightful discussions.

REFERENCES


Table II. Measured Performance Summary of the LDO.

<table>
<thead>
<tr>
<th>Input voltage range, Vₒₒ</th>
<th>1.43V – 3.3V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Regulated output voltage Vₒₒ</td>
<td>1.21V</td>
</tr>
<tr>
<td>Load current range, Iₒₒ</td>
<td>1mA – 100mA</td>
</tr>
<tr>
<td>Line Regulation, ΔVₒₒ/Vₒₒ</td>
<td>0.05 %/mV</td>
</tr>
<tr>
<td>Load Regulation, ΔVₒₒ/Iₒₒ</td>
<td>0.001 %/mA</td>
</tr>
<tr>
<td>Max Load Transient ΔVₒₒ</td>
<td>&lt; 120mV with Cₒₒ = 0.1µF</td>
</tr>
<tr>
<td>Dropout Voltage, Vₒₒ drop</td>
<td>45mV with Iₒₒ = 1mA, 220mV with Iₒₒ = 100mA</td>
</tr>
<tr>
<td>Power Supply Rejection Ratio, PSRR</td>
<td>–52.5dB at 100Hz, –45.2dB at 10kHz</td>
</tr>
<tr>
<td>Output Cap value Cₒₒ</td>
<td>0.1µF – 1µF</td>
</tr>
<tr>
<td>Output Cap type</td>
<td>Ceramic, MLCC</td>
</tr>
<tr>
<td>Power Good output, VₚＧ</td>
<td>Digital high @ 95% of Vₒₒ</td>
</tr>
<tr>
<td>Process</td>
<td>0.1µm CMOS 2P3M</td>
</tr>
<tr>
<td>Area</td>
<td>762µm x 284µm</td>
</tr>
</tbody>
</table>