FULLY INTEGRATED CURRENT-MODE SUBAPERTURE CENTROID
CIRCUITS AND PHASE RECONSTRUCTOR

BY

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DEDICATION

This thesis is dedicated to my parents, to my brothers, to my sisters and to my friend Philomena Midecha Mulera. Thank you for your support and encouragement.

I am thankful to my advisor, Paul Furth, and to his family for all the love that they have shown me throughout my master’s program. God bless you always.
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This has indeed been the most challenging time in my entire education; I have never felt so drained and tired. I am thankful to the Almighty Lord for leading me through this tempting period in my life.

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ABSTRACT

FULLY INTEGRATED CURRENT-MODE SUBAPERTURE CENTROID CIRCUITS AND PHASE RECONSTRUCTOR

BY

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New Mexico State University
Las Cruces, New Mexico, 2001

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Analog processing has higher possible bandwidth and, given that the metal oxide semiconductor (MOS) devices operate in the subthreshold region, power consumption is extremely low. Further, sensory data is in the analog domain and thus compatibility to higher-level analog signal processing blocks is guaranteed. There is no need for costly analog to digital (A/D) conversions.

The motivation behind this project is to come up with a single chip solution that will reconstruct the phase of an aberrated wave incident upon a surface. Lenslets focus the phase-tilt onto a spot. The purpose of our centroid circuit is to determine the
position of the focused spot. Signals from the centroid circuit are then processed and injected into a resistive grid, which does phase reconstruction.

Previously wave reconstruction was performed in four steps. Photons incident on a charge coupled device (CCD) or complimentary metal oxide semiconductor (CMOS) imager are focused onto a spot. Second a centroid circuit determines the location of the focused spot, say, along the $x$–axis. This location is proportional to the first derivative of the phase. Third, by taking the finite difference of two neighboring centroid circuits a signal proportional to the second derivative is computed. Fourth, this second derivative is injected into a resistive grid that performs phase reconstruction.

Here we combine all of these steps. We amplify a current generated by a CMOS imager, compute the second derivative and inject it directly into the resistive grid in one chip. Four large photodiodes, arranged as a quad cell, generate continuous photocurrents in the picoAmpere range. We use the translinear characteristics of MOS transistors operating in the subthreshold region to amplify each photocurrent and normalize them by the sum of the photocurrents in the quad cell. Thus, our centroid computation is independent of the absolute light intensity. The finite difference computation is achieved through current summation at the nodes on the resistive grid.

This work describes the design, analysis and characterization for two different approaches to the problem of computing the second derivative of the phase. We then
proceed to implement one of these solutions as an analog very large scale integrated (VLSI) circuit.
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1 INTRODUCTION

Compared to digital signal processing, analog signal processing is proving to be the way forward in large-scale neural computation. Analog processing has higher possible bandwidth and, given that the metal oxide semiconductor (MOS) devices operate in the subthreshold region, power consumption is extremely low. Further, sensory data is in the analog domain and thus compatibility to higher-level analog signal processing blocks is guaranteed eliminating the need for costly analog to digital (A/D) conversions. Finally, low power circuits implemented in subthreshold occupy small silicon area, thus leading to higher yield.

In this thesis, we start with determining the locations of spots focused by a lenslet array. We work in the current domain and use the translinear principle to amplify photocurrents detected by the photodetectors. We employ normalization to ensure that the centroid computation is independent of absolute light intensity. This work is entirely based on research previously published by Furth and Clark [Fur98]. Original contributions in this report are;

- We have integrated the Centroid computation and the second derivative on a single chip.
- We have also integrated the second derivative and phase reconstruction on a single chip.
- We have verified the operation and limitations of the translinear principle using a subthreshold current amplifier.
In chapter 2, we give a generalized comparison between the silicon retina and the biological retina. We review some of the major advances that have been made in the design of the silicon retina and mention their limitations. The resistive grid is ubiquitous to solutions that require spatial smoothing; thus, we talk about the behavior of the resistive grid. We also mention photodetectors that are available in an n-well process. We also review basic analogies for partial differential equations since they describe many naturally occurring systems. Finally since we are going to work in subthreshold we review the equations that describe the CMOS transistor in subthreshold.

In chapter 3, we describe in detail the fully integrated current-mode subaperture centroid circuits and phase reconstructor. We compare two solutions to the problem at hand; that is the, voltage-mode approach and the current-mode approach. We also do all the characterization of the circuits that are employed in this design.

In chapter 4, we go into the laboratory to verify that the cell is going to work. Using a digital prototype chip that we designed, layed out, fabricated and tested using the 0.5-μm AMI n-well process, we verify the operation of the basic translinear amplifier. Further we make a layout for the cell and the quad cell and perform layout versus schematic (LVS) on these cell-blocks.

Finally, chapter 5 provides a summary of the thesis and offers some ideas for advances in this area.
2 THE SILICON RETINA AND PARTIAL DIFFERENTIAL EQUATIONS

2.1 Introduction

The biological retina itself is incapable of distinguishing events. Signals generated by the retina have to be transmitted to the brain where they are interpreted or processed. The major goal of a silicon retina is to have a system that can generate real-time outputs that mimic the biological retina. The output of the silicon retina is analogous to the output of the ganglion cells in the retina in that it resembles the Laplacian filter. Charge coupled devices (CCD’s) are the predominant technology utilized for image capture. This is because of their high density, low noise, minimal nonuniformity, high sensitivity and relatively simple manufacturing process [Del96]. In addition, easy availability and reliability are other advantages. Major drawbacks of CCD’s are that they are serial devices, thus suited for display and transmission to televisions. Additionally they require numerous clocking devices and dedicated power supplies. Complimentary metal oxide semiconductor (CMOS) imagers are a desirable alternative because of their smaller size and lower power consumption, leading to reduced cost. Also they give an analog output that is compatible with analog signal processing circuits. Much research has been done on the design and implementation of silicon retinas.

Most natural systems can be modeled using partial differential equations. These natural systems can be modeled as dissipative, kinetic energy storing, and potential energy storing. There are two very distinct approaches to this problem, i.e.
the digital and the analog solution. The latter is a better option due to its fast speed and the parallel nature of the computation.

2.2 The silicon retina

2.2.1 Biological model

Signal flow in a biological retina model is shown below. First, light incident on photoreceptors is transduced to produce a signal that is proportional to the intensity.

Figure 2-1 Signal flow in the biological retina model based on Mead [89]
This signal then proceeds into the triad synapses, which contain the horizontal cells that compute spatial and temporal smoothing. The output is then transmitted to the bipolar cells that take the difference between the photoreceptors and the horizontal cells. The difference, which is digital in amplitude and analog in time [Haz94], is then transmitted to the retinal ganglion, which relays the electrical signals to the brain for interpretation. Of importance is the retina's capability to discern edges. The ideal silicon retina should be able to identify edges in scenes. The characteristic of the retina is the Mexican hat, which shows that the intensity fades away exponentially as we move away from the center of stimulation. A typical point spread for the silicon retina is shown in figure 2-2.

Figure 2-2 Typical point spread for the Mead retina [Coll94].
The Fourier transform of this signal yields a high pass solution as shown in figure 2-3. The high pass filtering operation is significant in detecting edges. This is clearly explained in [Coll94].

![Figure 2-3 FFT for figure 2-2 [Coll94].](image)

2.2.2 Artificial model

The artificial model of choice uses the analog approach to mimic the retina. Light incident on the photoreceptors is transduced to produce a current that is proportional to the logarithm of the intensity. Mead and coworkers implemented a logarithmic photoreceptor cell [Mead89] shown in figure 2-4. This cell consists of a logarithmic element (M1 and M2 diode connected) and a photo detector. It performs signal compression. The photo detector generates a very small current (pA), which makes the diode-connected transistors operate in the subthreshold region.
These PMOS devices operate in subthreshold thus the current is logarithmically related to the gate to source voltage. At this juncture it is worthwhile to mention other forms of photodetectors that may be fabricated in a standard n-well CMOS process. Photodetectors are the door-way to integrated image processing systems. They are generally realized using parasitic elements found in standard CMOS processes. Some examples of parasitic elements are illustrated in the figure 2-5. Some assumptions made for purposes of characterizing these parasitic elements; they have abrupt junctions, they have one-dimensional current flow, they have no degeneration, they have no recombination in depletion regions and they have no diffusion in the bulk substrate. Very large photodetectors show low mismatch. Phototransduction depends on the characteristic of the bulk semiconductor. A photodiode is formed by reverse biasing a region of n-type diffusion in the p-substrate. The photocurrent is proportional to the intensity of the incoming light. The
photodiode suffers from a large parasitic depletion capacitance that is proportional to the area of the reverse-biased $pn$ junction [Fur98].

A phototransistor occurs as a natural by product of the CMOS process. Electrons in the n-well gather at the base, this leads to a lower potential between the base and emitter thus leading to an easy flow of current from the emitter to the collector [Mead89].

![Diagram of photodetectors](image)

Figure 2-5 Possible photodetectors found in a standard n-well CMOS process [Ali97], (a)n-well photodiode, (b) n-well double photodiode,(c) substrate photodiode,(d) phototransistor.

Delbrück [Del96] implemented an adaptive photo detector circuit that can be used in massively parallel analog chips. The receptor provides a continuous time
output that has low gain for static signals and high gain for transient signals centered on the adaptation point.

The horizontal cell’s spatial smoothing effect is achieved using a resistive grid. The resistive grid is ubiquitous in analog solutions due to its simplicity. The basic structure of a one-dimensional resistive grid is shown in figure 2-6. One should note that as you move away from the location of stimulation the response fades, results in spatial smoothing.

![Figure 2-6 One dimensional resistive grid.](image)

Voltage decay in a resistive grid is computed using

\[ V_n = \lambda^n V_o \]  (2-1)

where

\[ \lambda = \frac{V_1}{V_o} = 1 + \frac{1}{2l^2} - \frac{l}{1 + \frac{1}{4l^2}} \]  (2-2)

and

\[ \frac{1}{l} = \sqrt{RG} \]  (2-3)

Carneiro[Car00] implemented an adaptive resistive grid. In his architecture voltages in adjacent nodes are used to vary the gate voltage of MOS transistors operating in the linear region. The resistance depends on the imaging application. For
image processing the resistance increases with increases in the absolute voltage between adjacent nodes while for solving partial differential equations the resistance decreases with increases in the absolute voltage between adjacent nodes. More generally, this approach has made possible the implementation of large-scale analog computational systems in a single chip [Ram94].

In an artificial retina we seek to mimic all the components of the retina i.e. photoreceptors, horizontal cells, bipolar cells and retinal ganglion cells. To achieve the horizontal cells’ temporal smoothing we can use a low-pass filter. The low pass filter can be implemented using an operational transconductance amplifier (OTA) and the parasitic capacitance of the resistive grid. The resistive grid accomplishes spatial smoothing. The effect of the bipolar cells is achieved by taking the difference between the photoreceptor cell output and the low-pass filter output (figure 2-7). This configuration achieves a high-pass filter effect, which is desired. This signal is then read out for processing.

The output voltage $V_{ph}$ of each photoreceptor controls a current, which is fed into a resistive layer of uniform resistance value $R$. 
The photoreceptor is linked to the grid cell by an OTA with the transconductance value $G$. An amplifier with gain $A$ takes the difference between the photoreceptor voltage, $V_{ph}$, and the cell node voltage, $V_{cell}$, to generate the cell’s output. The follower connected transconductance amplifier, together with the parasitic capacitance, $C$ of the cell’s center node, forms the follower integrator. The capacitor discharge rate is given by

$$C \frac{\partial V_{cell}}{\partial t} = I_b \tanh \left[ \frac{\kappa (V_{ph} - V_{cell})}{2V_t} \right]$$  \hspace{1cm} (2-4)

where $I_b$ is the bias current for the OTA, $\kappa$ is the subthreshold slope factor, typical values of $\kappa$ range from 0.7 to 0.9. $V_t = \frac{kT}{q}$ is the thermal voltage which is
approximately 25mV at room temperature. For small signals the tanh can be approximated as

$$C \frac{\partial V_{cell}}{\partial t} = G(V_{ph} - V_{cell})$$  \hspace{1cm} (2-5)$$

where $G = \frac{\kappa I_b}{2V_t}$ is the small signal transconductance value of the OTA. The above equation can be rewritten as

$$\frac{V_{cell}}{V_{ph}} = \frac{1}{\tau s + 1}$$ \hspace{1cm} (2-6)$$

where $\tau = \frac{C}{G}$.

Consider the voltage gain, $A$ of the output amplifier, taking the difference between the $V_{ph}$ and the OTA output, a differentiator is formed. The cell’s output signal is now written

$$V_{out} = A(V_{ph} - V_{cell}) = AV_{ph}(1 - \frac{1}{\tau s + 1}) = \frac{A\tau}{\tau s + 1}V_{ph}$$ \hspace{1cm} (2-7)$$

The functionality of the cell can be illustrated in figure 2-8 and 2-9. One should note the high pass effect that performs edge detection (figure 2-8) and the low pass filter response to an impulse signal that performs temporal smoothing (figure 2-9).
Problems that imagers face are regularization and discontinuities. Regularization is the process of extracting three-dimensional information from a two-dimensional scene. It is an ill posed problem. Discontinuities occur at boundaries of objects in a scene. A silicon retina should be able to detect sharp changes at the boundaries, i.e. perform edge detection. The characteristic of a low pass filter is smoothing, the effect of the low pass filter can clearly be seen in figure 2-8. A high pass filter has a spiking characteristic; this is edge detection. Edge detection is evident in figure 2-9.
Partial differential equations are mathematical solutions to naturally occurring systems. The three naturally occurring systems are dissipative, kinetic energy storing, and potential energy storing. These naturally occurring systems are often mechanical; however, we want to build analogous systems using electrical systems. Dissipative elements can be mimicked using resistors. Potential energy storing elements can be mimicked using capacitors, while kinetic energy storing elements are mimicked using inductors. Generally, partial differential equations are grouped into three categories, i.e., parabolic, elliptic, and hyperbolic. The good news is that all these categories can be
solved using the resistive grid [Ram94]. Some resistive grid configurations that may be used to solve partial differential equations are shown in figure 2-10.

![Resistive Grid Configurations](image)

Figure 2-10 Circuit implementation for (a) Elliptic Equation (b) Heat Equation and (c) Wave Equation (FDNR-frequency dependant negative resistance) [Car00].

As an example let us show that the four element resistive grid can be used to solve a partial differential equation. The partial differential equation most relevant to this thesis is the Poisson or Elliptic equation whose form is

\[
\frac{\partial^2 u}{\partial x^2} + \frac{\partial^2 u}{\partial y^2} = \rho(x, y)
\]

(2-8)

where \( u(x,y) \) is an unknown spatial function in variable \( x \) and \( y \) and \( \rho(x,y) \) is the forcing function. Let \( u_{k,l} \) be a discrete approximation of the unknown function \( u(x,y) \) where \( k = 1,2,\ldots \), and \( l = 1,2,3,\ldots \). A finite second order difference equation can be written as

\[
\frac{\partial^2 u_{k,l}}{\partial x^2} = \frac{[u_{k+1,l} - u_{k,l}] - [u_{k,l} - u_{k-1,l}]}{\Delta^2}
\]

(2-9)
where $\Delta$ is the grid spacing. Thus $k$ is the number of $\Delta$’s along the $x$-axis and $l$ is the number of $\Delta$’s along the $y$-axis. Substituting into Poisson’s equation we obtain

$$
\frac{[u_{k+l,j} - u_{k,j}]}{\Delta^2} + \frac{[u_{k,j+1} - u_{k,j}]}{\Delta^2} = \Delta^2 \rho(x,y) \tag{2-10}
$$

$$
u_{k+l,j} + u_{k,j+1} + u_{k,j-1} - 4u_{k,j} = \Delta^2 \rho(x,y) \tag{2-11}
$$

Now for the resistive grid shown in figure 2-10(a), assume that the center node is labeled zero. Using Kirchhoff’s current law and summing the currents at node 0 we have

$$
\frac{V_1 - V_0}{R_1} + \frac{V_2 - V_0}{R_2} + \frac{V_3 - V_0}{R_3} + \frac{V_4 - V_0}{R_4} = I \tag{2-12}
$$

and

$$V_1 + V_2 + V_3 + V_4 - 4V_0 = RI \tag{2-12}
$$

assuming $R_1 = R_2 = R_3 = R_4 = R$.

The expression above is similar to that obtained from the difference equation solution. Other equations may be represented using analogies shown in figure 2.8 (b) and (c)[Car00].

2.4 Subthreshold operation

The increasing need for low power and low current circuits has led to more utilization of MOS transistors operating in subthreshold. The main problem that plagues circuits designed to operate in the subthreshold region is matching. Since the drain current is exponentially related to the gate to source voltage, any mismatch in
these voltages can cause significant differences in the drain current [Bak98]. This region of operation is also known as weak inversion.

In the subthreshold region, the characteristics of the MOS transistor are similar to those of the bipolar junction transistor (BJT). At voltages below the threshold we observe that MOS devices are translinear, i.e. the device-current has an exponential dependency on the gate voltage [And96]. For an NMOS transistor the subthreshold current $I_{DS}$ is given by equation (2-14) while for the PMOS all the potentials are sign reversed.

$$I_{DS} = I_o \frac{W}{L} e^{\frac{\kappa V_{GS}}{V_T}} \left( e^{\frac{V_{SB}}{V_T}} - e^{\frac{V_{DS}}{V_T}} \right) \tag{2-13}$$

where $I_o$ is the zero bias current, $\kappa$ is the subthreshold slope coefficient [And96]

$$\kappa = \frac{C_{OX}}{C_{OX} + C_{Dep}} \tag{2-14}$$

$C_{OX}$ is the oxide capacitance while $C_{Dep}$ is the depletion capacitance. $V_T$ is the thermal voltage, $S = \frac{W}{L}$ and other voltages are by convention.

If the transistor operates in the saturation region i.e. $V_{DS} \geq 4V_T$ and $V_S = V_B$ that is $V_{SB} = 0$ then the current through the NMOS device becomes

$$I_D = S I_o e^{\frac{\kappa V_{GS}}{V_T}} \tag{2-15}$$
Since $I_o$ is very small, the available current to charge and discharge capacitances is also small resulting in poor frequency performance. Square transistors in the subthreshold region exhibit currents in the pico to nano-ampere range.

Transistors operating in the subthreshold region are more susceptible to parametric mismatch. Consider a simple current mirror, from [Bak98] we see that when operating above threshold ($V_{GS} - V_{t} > 200\text{mV}$) the output current mismatch is given by

$$\frac{I_{out}}{I_{in}} = 1 - \frac{2\Delta V_t}{V_{GS} - V_t} \quad (2-16)$$

where $V_t$ is the threshold voltage of the transistor.

The equation above shows that a decrease in the gate to source voltage will lead to greater output current mismatch due to threshold variations. Other mismatches in transconductance, lambda and drain to source voltage also come into play. Also because of the exponential dependence of $I_{DS}$ on gate to source voltage, very small variations in $V_t$ will produce a large variation in $I_{DS}$. A one percent change in $V_t$ yields nearly a twenty percent change in $I_{DS}$. It is unrealistic to expect control of $V_t$ below one percent [Mic92].

2.5 Problem formulation

Delbrück [Del96] implemented an adaptive photoreceptor circuit. This circuit incorporates an adaptive element and provides a continuous–time output that has low gain for static signals and high gain for transient signals centered on the adaptation
point. In [Fur98] photo detection is achieved using the Mead photoreceptor and an active feedback photoreceptor element as shown in figure 2-12.

In figure 2-11(a) we convert the input photocurrent into a voltage. The photodiode generates a small current that sends M2 into subthreshold. An increase in current implies a corresponding increase of $V_{gs2}$, thus an increase of $V_{\text{photo}}$ relative to $V_{SS}$. We should note that the current through M2 is exponentially dependant on $V_{gs2}$; we are thus compressing the input photocurrent. The feedback mechanism through M1 and Mcasc decreases the input resistance seen by the photodiode, therefore increasing the bandwidth of the detector. A small increase in $I_{\text{photo}}$ causes the voltage at the source of M2 to be pulled down. As a result $V_{\text{photo}}$ goes up by the amplifier.
gain. Since M2 is connected as a source follower, the voltage at the source of M2 will follow the increase in $V_{\text{photo}}$. In that way the voltage at $V_{in}$ is stabilized. In figure 2-11(b) we convert the input photocurrent into a voltage using a photodiode or a phototransistor. $V_{\text{casc}}$ controls the amount of current that will flow through the circuit. $V_{\text{photo}}$ is exponentially related to the current $I_{\text{photo}}$ flowing through Mcasc.

Carneiro [Car00] implemented an adaptive cell for resistive grid applications. Here inter-node resistance is varied depending on adjacent nodal voltages. A feasible problem formulation is to combine the adaptive photoreceptor and the adaptive resistive grid. This system should be capable of image processing and solving partial differential equations depending on the logic selection.

In this thesis we focus on the subaperture centroid circuits. Furth and Clark [Fur98] have implemented a circuit that is able to detect the position of a spot focused by the lenslet. They have implemented a solution that uses photocurrents generated by a photoreceptor to locate the position of a spot. In their work only the first derivative is integrated on the same chip. The second derivative computation is done externally. In this paper we seek to locate the position of the focused spot by using a quad cell. Here the location of the image centroid is never explicitly computed. We combine all four steps previously in [Fur98] so that we are able to generate a current that will be injected directly into the resistive grid in one step. We operate in the current-mode and use translinear characteristics of MOS transistors to amplify
photocurrents, which we inject directly into a resistive grid. This process is explained in the following chapter.
3 ALTERNATE SUBAPERTURE CENTROID CIRCUITS

3.1 Introduction

The entire system that we design should be able to estimate the phase of a wavefront [Fur99]. Lenslets focus phase aberrations onto photodetectors that generate currents that are eventually injected into a resistive grid for phase reconstruction.

One objective of this research is to demonstrate the feasibility of the VLSI implementation of subaperture centroid circuits. Furth and Clark [Fur98] give a solution to the problem. However, working directly in the current domain and by taking the difference of neighboring centroid current values we can compute a signal that is proportional to the second derivative of the phase of the incident light, as illustrated in figure 3-1.

The location of the focused spot should be independent of intensity. Thus, if the intensity of an entire scene changes, the location of the centroid should remain the same. In this chapter we explore two distinct solutions for computation of an image centroid: in the first solution, currents transduced from the centroid are converted into voltages. These voltages are then fed into a quad differential amplifier, which generates a bi-directional current proportional to the second derivative of the phase of the incident light. This bi-directional current is then injected into a resistive grid from whence we are able to reconstruct the phase. In the second solution, photocurrents are amplified, normalized and injected directly into the resistive grid.
Analog signal processing is better than digital for high bandwidth, low precision, non-linear signal processing. Transistors operate in the subthreshold region, where currents are in the pico-ampere to nano-ampere range for square devices. MOS devices operated in subthreshold have extremely low power dissipation. Since subthreshold MOS devices are translinear, i.e. the device-current has exponential dependency on the gate.

Figure 3-1 One-dimensional diagram of fully integrated current-mode subaperture centroid circuits and phase reconstructor
voltage [And96] this leads to a small voltage swing and hence decreasing power delay product. Also, as supply voltages become lower and lower, subthreshold circuits may emerge as the dominant approach because the gate to source voltages and the drain to source saturation voltages are minimum in this region.

3.2 Subaperture centroid solution 1: Quad Differential Amplifier

In [Fur98] each centroid circuit consists of four photo sensors arranged in a square pattern and two differencing circuits as shown in figure 3-2. Differencing circuits are used to compute the location of the focused spot relative to the center of the square pattern, i.e. in the $x$ and $y$ directions. The computation is done using the partial differential equations show below

$$\frac{\partial u}{\partial x} = G[(V_{ph1,1} + V_{ph2,1}) - (V_{ph1,2} + V_{ph2,2})] = i_x$$  \hspace{1cm} (3-1)

$$\frac{\partial u}{\partial y} = G[(V_{ph1,1} + V_{ph1,2}) - (V_{ph2,1} + V_{ph2,2})] = i_y$$  \hspace{1cm} (3-2)

where $V_{phx,y}$ is the voltage generated by the photocurrent from sensor $[x,y]$ and $G$ is the transconductance of the differencing amplifier. The current $i_x$ is the local estimate of the first derivative in the $x$-direction; $i_y$ is the local estimate of the first derivative in the $y$-direction.

In order to produce a local estimate of the second derivative of the incident light we compute the difference between the $x$-axis current in the local centroid, say
\( i_{x1} \), and the \( x \)-axis current from the neighboring centroid, say \( i_{x2} \). We do likewise for the \( y \) argument.

\[
\frac{\partial^2 u}{\partial x^2} = i_{x1} - i_{x2} = i_{\text{xinj}} \quad (3-3)
\]

\[
\frac{\partial^2 u}{\partial y^2} = i_{y1} - i_{y2} = i_{\text{yinj}} \quad (3-4)
\]

Figure 3-2 Quad photodetectors loads (Current to voltage converters) and double differential amplifiers to compute the image centroid.
The second difference computation is computed off chip, then it is injected into the Poisson equation solver implemented as a resistive grid. Summing (3-3) and (3-4) we get

\[
\frac{\partial^2 u}{\partial x^2} + \frac{\partial^2 u}{\partial y^2} \approx i_{\text{inj}} + i_{\text{inj}} = \rho(x, y)
\]  

Equation (3-5) is Poisson’s equation that is solved easily using the resistive grid as discussed in chapter two.

In this thesis we seek to achieve the computation of equations 3-1 through 3-4 directly without going through two differencing circuits. As was mentioned earlier we may choose to amplify the photocurrents and then inject them directly into the Poisson equation solver or we may choose to convert the photocurrents into voltages. The latter solution is attractive because using the translinear principle the constant of proportionality can be made to be approximately the amplifier bias current divided by the total photocurrent [Fur98]. Thus the computation of the image centroid is independent of the absolute light intensity. In this scheme the basic centroid consists of four large photo sensors arranged in a square pattern and a quad differencing circuit for every two centroid circuits, as shown in figure 3-3.

Referring to figure 3-3, the location of the image centroid is never explicitly computed. Along the \( x \)-axis we take the difference between the voltages from photo sensors [1,1] [1,2] [2,3] [2,4] and the voltages from photo sensors [1,3] [1,4] [2,1] [2,2]. This difference ideally gives us the second derivative, which is then injected into the Poisson equation solver.
\[
\frac{\partial^2 u}{\partial x^2} = G[(V_{ph1,1} + V_{ph1,2} + V_{ph2,3} + V_{ph2,4}) - (V_{ph1,3} + V_{ph1,4} + V_{ph2,1} + V_{ph2,2})] = i_{xinj} \quad (3-6)
\]

\[
\frac{\partial^2 u}{\partial y^2} = G[(V_{ph1,1} + V_{ph1,2} + V_{ph1,1} + V_{ph1,2}) - (V_{ph2,1} + V_{ph2,2}, V_{ph1,1} + V_{ph1,2})] = i_{yinj} \quad (3-7)
\]

where \(G\) is the transconductance of the quad-differencing amplifier.

With this scheme we have substantially reduced circuitry. We also do not have as many computations on the photocurrent-input as was done in [Fur98]. The diagram describing equation 3-6 is shown in figure 3-3, while that describing equation 3-7 is shown in figure 3-4.

![Diagram](image)

**Figure 3-3**  Two quad photodetectors, voltage-to-current converters and a quad differential amplifier \(x\)-axis configuration.
Figure 3-4 Two quad photodetectors, voltage-to-current converters and a quad differential amplifier y-axis configuration.

3.2.1 Photocurrent load

Light is transduced into a current using a reverse biased photodiode. We need to either amplify this current or convert it into a voltage using a load. The circuit that does this operation should be a compression circuit, so that we can deal with inputs that have a large dynamic range. Currents generated by the photodiode are in the pico-Ampere range. Devices driven by this current are thus in subthreshold. A schematic of the active load used in this design to convert photocurrent into voltages is shown in figure 3-5. It is similar to the active load in [Del96]. Delbrück and coworkers [Del96] also have a similar circuit that incorporates an adaptive element. In Delbrück's work [Del96] his circuit has high gain for transient signals and low gain for static signals, i.e. it is somewhat invariant to absolute light intensity.
In this circuit we convert the input photocurrent into a voltage. The photodiode generates a small current that sends M1 into subthreshold. An increase in current implies a corresponding increase of $V_{gs1}$, thus an increase of $V_{photo}$ relative to $V_{ss}$. We should note that the current through M1 is exponentially dependent on $V_{gs1}$; we are thus compressing the input photocurrent. The feedback mechanism through M2 and Mcasc decreases the input resistance seen by the photodiode, therefore increasing the bandwidth of the detector. A small increase in $I_{photo}$ causes the voltage at $V_{in}$ to be pulled down. As a result $V_{photo}$ goes up by the amplifier gain. Since M1 is
connected as a source follower $V_{in}$ will follow the increase in $V_{photo}$. In that way the voltage at $V_{in}$ is stabilized.

As CMOS feature sizes become smaller and smaller, analog CMOS circuits have been forced to operate with continuously decreasing supply voltages [Ram98]. In this thesis the lowest $V_{DD}$ is 2.5V with a 0V $V_{SS}$, while with a split power supply we are operating at +1.25V and –1.25V. Simulations for the schematic of figure 3-5 from T-Spice are shown in figure 3-6.

![Figure 3-6 Simulations from active load photodector $V_{DD} = 1.25$, $V_{SS} = -1.25$, $I_{bias} = 1\mu A$.](image-url)

Figure 3-6 Simulations from active load photodector $V_{DD} = 1.25$, $V_{SS} = -1.25$, $I_{bias} = 1\mu A$. 
Here we sweep the ideal input photocurrent from 0.1nA to 10nA and observe the output voltage, $V_{\text{photo}}$. We also set $I_{\text{bias}}$ to 1µA using a bias resistor (1.4MΩ) to $V_{SS}$. Figure 3-6 shows us that the change in $V_{\text{photo}}$ is small as the current varies. So we have converted the input photocurrent into a voltage and have also logarithmically compressed it. For a change in photocurrent from 0.1nA to 1nA and from 1nA to 10nA, the photo voltage changes by approximately 80mV/decade. This corresponds to a subthreshold slope factor of $\kappa \approx 0.72$. One thing to note is that since $V_{\text{photo}}$ is connected directly to a gate terminal, we do not draw any current from the active load circuit.

### 3.2.2 Differential pair

Photo voltages generated from the active load are then connected to a differential circuit. We have four voltages; we need a differential circuit that has four negative input terminals and four positive input terminals. A schematic of this quad differential pair is shown in figure 3-7.

A low-voltage current mirror is used in order to get higher output resistance. The low voltage cascode current mirror [Bak98] enables the circuit to operate at low supply voltages and have maximum output swing. $V_{\text{cas}}$ biases M11 and M12. One disadvantage of using the cascode current mirror is increased area; another is increased power through the transistors that will generate $V_{\text{cas}}$. On the other hand these transistors will be operating in subthreshold, so this power will be very low.
This differential amplifier gives an output current that depends on the differential input voltages. When all the inputs to the positive terminal are greater than the inputs to the negative terminal we should expect a positive output current.

Using Kirchhoff’s law at node A and the equation \( I_{DS} = I_o e^{\frac{V_{GS}}{V_T}} \) for MOS transistor devices operating in subthreshold; we can show [Mead89]

\[
I_{\text{out}} = I_1 - I_2 = I_{\text{bias}} \tanh \left( \frac{\kappa(v_1 - v_2)}{2V_T} \right) \tag{3-8}
\]

Where \( v_1 = v_{+1} = v_{+2} = v_{+3} = v_{+4} \) and \( v_2 = v_{-1} = v_{-2} = v_{-3} = v_{-4} \). That is all the positive inputs are tied to \( v_1 \) and all negative terminals are tied to \( v_2 \). \( V_T \) is the thermal
voltage. The more general case of \( v_1 \neq v_{+1} \neq v_{+2} \neq v_{+3} \neq v_{+4} \) and \( v_2 \neq v_{-1} \neq v_{-2} \neq v_{-3} \neq v_{-4} \) yields an exponential relationship between all eight input voltages and the output current. \( \kappa \) is the subthreshold slope factor.

As the differential voltage \( v_1 - v_2 \) increases the output current saturates at \( I_{\text{bias}} \). Figure 3-8 obtained from simulating the quad differential amplifier, suggests a positive output current when \( v_1 \) is greater than \( v_2 \).

Figure 3-8 Output current of the quad-differential pair when all the positive terminals are tied together and all the negative terminals are tied together. \( V_{DD} = 1.25V, V_{SS} = -1.25V, I_{\text{bias}} = 13nA \).
In the simulation we set a common-mode input at 500mV, and configured a differential voltage by making the input voltage into the negative terminal to be dependant on the voltage at the positive terminal, with a gain of minus one. This setup allows us to plot the differential voltage versus the output current.

Figure 3-8 shows that as we apply a differential voltage from -500mV to 500mV the output current swings from -13nA to 13nA. Next, we simulated the maximum and minimum voltage swings. Maximum and minimum output voltages are of importance to us because we want the output current to be stable over a wide range of output voltages. A simulation showing the maximum and minimum voltages is shown in figure 3-9. From the graph the max output voltage is 1.20V while the minimum is -0.70V for \( V_{DD} = 1.25V, \ V_{SS} = -1.25V \).

The minimum voltage does not hit -1.25V. We may get closer to -1.25V by increasing the \( W \) of the differential pair or the \( W \) of the current mirror that generates the bias current \( I_{bias} \). The gain is the maximum slope, which is 94V/V.

The gain of the quad differential pair from one pair of the differential inputs is given by

\[
A_v = g_m * R_{out} \tag{3-9}
\]

where \( g_m \) is the transconductance of each differential pair and \( R_{out} \) is given by

\[
R_{out} = \left( g_{m12} r_{ro12} r_{o14} \right) \parallel r_{tot} \tag{3-10}
\]
Figure 3-9 Maximum and minimum output voltage swings when all the positive terminals are tied together and all the negative terminals are tied together and the negative terminal is tied to ground while the positive terminal is swept from –0.5V to 0.5V. $V_{DD} = 1.25V$ $V_{SS} = -1.25V$, $I_{bias} = 13nA$.

and

$$r_{sat} = \frac{1}{\lambda I_2}$$

$I_2$ is the sum of the currents through M7, M8, M9 and M10 which is approximately $\frac{I_{bias}}{2}$ in steady state.
3.3 Subaperture Centroid Solution 2: Current Amplification

In this section, current amplification will be considered. In this thesis we opted to implement this solution due to its compactness.

Currents generated by the photo detector are in the pico-ampere range. Using a configuration in which all the devices are operating in subthreshold we first amplify this pico-ampere current and inject it directly into the resistive grid. Using Kirchhoff’s current law, i.e. summation and subtraction of currents at the node, we are able to reconstruct the phase of the wavefront. As was mentioned earlier, the second derivative can be computed by taking the difference between the centroid currents at neighboring quad cells. Equation (3-11) shows the unnormalized second derivative along the x-axis while equation (3-12) shows the same along the y-axis. The resistive grid then yields the solution to the Poisson’s equation, i.e. reconstructs the wavefront.

\[
\frac{\partial^2 u}{\partial x^2} = (I_{out11} + I_{out12} + I_{out23} + I_{out24}) - (I_{out13} + I_{out14} + I_{out21} + I_{out22})
\]  \hspace{1cm} (3-11)

\[
\frac{\partial^2 u}{\partial x^2} = (I_{out11} + I_{out13} + I_{out23} + I_{out34}) - (I_{out12} + I_{out14} + I_{out31} + I_{out33})
\]  \hspace{1cm} (3-12)

Figure 3-10 shows how currents are injected into the resistive grid. Consider node \( V_x \). Currents \( I_{out11}, I_{out12}, I_{out23}, I_{out24} \) are amplified photocurrents generated by sensor amplifiers \([1,1],[1,2],[2,3],[2,4]\) respectively. Using PMOS low voltage current mirrors these currents are sourced into node \( V_x \).
Figure 3-10 Current injection into a 2x2 resistive grid along the x-axis injection.

Next, currents \( I_{out1,3} \), \( I_{out1,4} \), \( I_{out2,1} \) and \( I_{out2,2} \) are amplified photocurrents generated by sensor amplifiers [1,3],[1,4],[2,1] and [2,2] respectively. Using NMOS low voltage current mirrors these currents are sunk out of node \( V_x \).

Along the y-axis consider node \( V_y \) in figure 3-11, currents \( I_{out1,1} \), \( I_{out1,3} \), \( I_{out3,2} \) and \( I_{out3,4} \) are amplified photocurrents generated by sensor amplifiers [1,1],[1,3],[3,2] and [3,4] respectively. Using PMOS low voltage current mirrors these currents are sourced into node \( V_y \). Also, currents \( I_{out1,2} \), \( I_{out1,4} \), \( I_{out3,1} \) and \( I_{out3,3} \) are amplified photocurrents generated by sensor amplifiers [1,2],[1,4],[3,1] and [3,3] respectively. Using NMOS low voltage current mirrors these currents are sunk out of node \( V_y \). The linear resistor value between read out nodes is 100Ω however we need to split this value into two so that we may get access to nodes \( V_x \) and \( V_y \).
Figure 3-11 Current injection into a 2x2 resistive grid along the $y$-axis injection

3.3.1 Translinear Current Amplifier

In designing a current amplifier we make use of the translinear loop principle [And96] which states that, “In a closed loop containing an equal number of oppositely connected translinear elements, the product of the normalized currents in the elements connected in the CW (Clockwise) direction is equal to the corresponding product for
the elements in the CCW (Counter clockwise) direction.” This principle should hold as long as the source to bulk voltage is made equal to zero or constant [Ter99].

A simple current mirror with all the devices operating in subthreshold can be used to illustrate the translinear loop principle. M1 and M2 in figure 3-12 form a translinear loop [Raf00]. They are both NMOS transistors and they have their bulk and source terminals shorted to ground. Figure 3-12 shows a schematic for a simple current mirror configuration.

![Figure 3-12 Simple current Mirror](image)

Using the translinear principle we expect the current through M1 to equal that through M2. Applying the translinear loop principle to this current mirror operating in subthreshold region, we notice that there are two oppositely connected translinear elements. Summing the voltages around this loop yields

\[ \sum_{CW} - \sum_{CCW} = V_1 - V_2 = 0 \]  

But from chapter two we found that \[ V_{GS} = \frac{V_t}{\kappa} \ln \left( \frac{I_D}{S I_o} \right) \], where \[ S = \frac{W}{L} \].

Assuming that \( \kappa_1 = \kappa_2 \) and that the device dimensions are equal, it follows that the
relation \( I_1 = I_2 \) holds. From this derivation it follows that we can use the translinear principle in the current amplifier. A schematic for the current amplifier is shown in figure 3-13. Looking at the loop \( V_{ss} \cdot A \cdot B \cdot C \cdot V_{ss} \) we are able to generate the following relation:

\[
\sum CW - \sum CCW = V_2 + V_1 - V_3 - V_4 = 0 \quad (3-14)
\]

and knowing that the gate-to-source voltages are given by equation(2-11), it follows then that

\[
\frac{V_T}{\kappa} \left[ \ln \left( \frac{I_1}{SI_o} \right) + \ln \left( \frac{I_2}{SI_o} \right) - \ln \left( \frac{I_3}{SI_o} \right) - \ln \left( \frac{I_4}{SI_o} \right) \right] = 0 \quad (3-15)
\]

\[
\ln \left( \frac{I_1 I_2}{SI_o} \right) = \ln \left( \frac{I_3 I_4}{SI_o} \right) \quad (3-16)
\]

Similarly assuming \( \kappa_1 = \kappa_2 = \kappa_3 = \kappa_4 \) and that the device dimensions are similar it follows that \( I_1 I_2 = I_3 I_4 \) or \( I_4 = I_{out} = \frac{I_1 I_2}{I_3} \).

In order to obtain a good gain we have to make the normalizing current \( I_3 \) small, while the scaling current \( I_2 \) should be large. Here all the dimensions of the transistors in the translinear loop must be equal. This is an attempt at reducing the effect of Kappa, \( \kappa \). Notice that M2 and M4 both have there back-gate terminal, the bulk connected to \( V_{ss} \) thus \( V_{SB} = 0 \). Also M1 and M3 have \( V_{SB} \neq 0 \). We are going to analyze the effect later.
3.4 Simulation

Transistors are sized so that they are able to source and sink the desired currents. We also choose the same W/L ratios for all the transistors in the translinear loop so that our assumptions in equation (3-16) may hold. MOS models in appendix A as used for all the simulations. Figure 3-13 was then modified to incorporate current mirrors, as shown in figure 3-14. \( V_{DD} \) was set to +1.25V while \( V_{SS} \) was set to –1.25V. \( I_1 \) was varied from 0.1pA to 9.9pA. \( I_2 \) was set to 10nA while \( I_3 \) was set to 100pA. Applying the translinear principle

\[
I_4 = I_{outp} = I_{outn} = \frac{I_1I_2}{I_3} \quad (3-17)
\]
the current gain is \( \frac{10\text{nA}}{100\text{pA}} = 100\text{A/A} \) thus we expect \( I_{\text{outn}} \) and \( I_{\text{outp}} \) to vary from 10\text{pA} to 990\text{pA}.

![Diagram of simple current amplifier](image)

Figure 3-14 Simple current amplifier of figure 3-12 with current mirrors.

We then simulated the schematic of figure 3-14. The results are shown in figure 3-15. From figure 3-15 it is clear that the gain is much higher than expected. Our theory predicted a maximum output current of 990\text{pA}; however, simulations show a maximum output current of about 2.5\text{nA}. Also the current from the PMOS current mirror is greater than that from the NMOS current mirror because of the Early effect.
Figure 3-15 Output current as a function of the input photocurrent for the translinear amplifier. $V_{DD} = +1.25$, $V_{SS} = -1.25$, $I_2 = 10\text{nA}$ and $I_3 = 100\text{pA}$.

In order to increase output resistance we choose to cascode every current mirror. Now, we expect the PMOS and NMOS output currents to be equal. Mcasc1 in figure 3-15 is used to prevent the Miller effect, i.e. it isolates node D from node B. It provides a low input resistance at node D and a high one at B [Greg99]. All cascode devices in figure 3-15 i.e. M9-M13 and M19 –M23 have $\frac{W}{L} = \frac{20}{3}$. The output current mirrors now have a higher output resistance so they are able to provide a stable current over a wide range of voltages.
Figure 3-16 Translinear current amplifier with low-voltage current mirrors.

Though this modification has positive results, it is at a cost. Cascode transistors almost double the number of transistors. In addition they have to be biased and this implies that we need two additional external pins for setting the bias voltages for the PMOS and NMOS cascode transistors. The circuit in figure 3-16 was then simulated. Results obtained from this alteration are plotted in figure 3-17.

Referring to figure 3-17 output current from the NMOS current mirrors exactly equals that of the PMOS current mirrors. We have introduced a 50pA offset for clarity. The measured gain appears to be slightly closer to the ideal gain, that is, the maximum output current has been reduced from 2.5nA to 2.1nA. However from
figure 3-17 we should note that the error is still very large. The slope should be approximately given by

\[ \frac{I_2}{I_3} = \frac{10nA}{100pA} = 100 \]  

(3-18)

Figure 3-17 shows a simulated slope of approximately 200A/A. Performing error analysis we obtain a percentage error of 100%, which is unacceptable. This error is possibly because the transistor models have not been characterized at these small currents below approximately 30pA. The results obtained in figure 3-17 are very
disturbing. Thus, a keen look into the mathematics, including all the parameters that we had assumed as being similar for all the transistors, are taken into consideration in Appendix B. Using figure 3-13, we see that M2 and M4 have zero bulk-to-source voltages. Thus we conclude $\kappa_2 = \kappa_4$. On the other hand M1 and M3 have nonzero bulk-to-source voltages. Therefore $\kappa_1, \kappa_3 > \kappa_2 = \kappa_4$. In general, $\kappa$ increases as bulk-to-source voltage increases. This phenomenon is known as the body effect. Furthermore, since the source to bulk voltage for M3 is less than the source to bulk voltage of M1 we choose $\kappa_1$ greater than $\kappa_3$. Assuming plausible values of $\kappa_2 = \kappa_4 = 0.7$ and $\kappa_1 = 0.76$ and $\kappa_3 = 0.75$, from the results in Appendix B the theoretical current gain should decrease by 28% to give $I_4 = 0.709\text{nA}$ as shown in figure 3-17. Thus, we may not attribute the increase in gain from the simulation to variations in $\kappa$.

Andreou [And96] suggests that setting the bulk voltage to all the MOS transistors in the translinear loop to a voltage below that of the source voltage will reduce variations $\kappa$. Using PMOS devices can be an advantage since we are able to connect the bulk to the source and thus eliminate body effect. However, laying out devices in independent wells is area intensive and increases parasitic capacitances at internal nodes. Having all these uncertainties, we decided to test the translinear current amplifier in the laboratory. Results obtained from testing were promising and they are discussed in chapter four.
The next step is to demonstrate that this scheme is going to work as proposed in the introduction. We inject the amplified current into a 2x2 resistive grid. Initially we set up our experiment to emulate the approach of Furth and Clark [Fur98]. We used a single centroid as shown in figure 3-2 in section 3.2. In our simulation we employed two quad cells as shown in figure 3-18.

![Figure 3-18 Current injection for the current-mode second derivative scheme (x-axis)](image)

For the x-direction, we hooked an ammeter to node $V_x$ and sourced amplified currents from sensor [1,1] [1,2] [2,3] and [2,4] into this node. We also sunk amplified currents from this node using sensors [1,3] [1,4] [2,1] and [2,2]. Using Kirchhoff’s current law, the current flowing through the Ammeter is the difference between the currents going into and out of node $V_x$. Measurements from this set up should show that there is no activity at node $V_y$, this is because we are not sinking or sourcing any current into this node thus simulations should also show that there is no activity at this node.
Similarly for the $y$-direction, we hooked an ammeter to node $V_y$ and sourced currents from sensors [1,1] [1,3] [3,2] and [3,4] into this node. We also sunk currents from this node using sensors [1,2] [1,4] [3,1] and [3,3] as shown in figure 3-19.

Referring to figure 3-18 photocurrents going into amplifiers [1,1] [1,2] [2,3] and [2,4] are varied in the same direction while currents going into amplifiers [1,3] [1,4] [2,1] and [2,2] are all varied in the same direction but opposite to amplifiers [1,1] [1,2] [2,3] and [2,4]. With this kind of set up we expect the current to vary only along the $x$-axis. Also for the simulation setup of figure 3-19 we should expect current to vary only the $y$-axis. We have not included simulations for figure 3-19 because they are implied from the simulations in figure 3-20.
Figure 3-20 Plot of output current along the x-axis

y-axis should show no variations. Results are shown in figure 3-20. The results obtained are concurrent to theory. From the simulated results we may deduce that for

\[
\left( I_{\text{photo11}} + I_{\text{photo12}} + I_{\text{photo23}} + I_{\text{photo24}} \right) \text{ greater than } \left( I_{\text{photo13}} + I_{\text{photo14}} + I_{\text{photo21}} + I_{\text{photo22}} \right)
\]

we have a positive output current while for the reverse we have a more negative current.

We then attach the sense amplifiers to the resistive grid. Initially a 2x2 grid is used. Based on work by Meitzler [Meit93] we expect the simulator not to converge for much larger dimensions. A block diagram of a 2x2 implementation is shown in figure 3-21.
Figure 3-21 Quad cells and a 2x2 resistive grid with node labels.

As shown in figure 3-21 all boundary voltages are fixed to ground. We select a value for $R_1$ equal to 50MΩ. We want to observe the labeled nodes as we vary the photocurrents into the sense amplifiers. First, we make all photocurrents to vary in the same direction. This represents a situation where no phase aberration has been detected. For this case we expect the voltage at all the nodes remain constant. We varied the photocurrent [1,1] from 0.1pA to 9.9pA and photocurrent[1,1] is the same as all the other photocurrents. We then observed the voltages at nodes
Figure 3-21 shows node voltages for all the labeled nodes.

Figure 3-22 Node voltages for all labeled nodes for figure 3-20.

The results obtained in figure 3-22 are concurrent with the theory. First all the voltages at the nodes of interest are equal. Second, the total variation is about 300µV, which is very small.

Next we make a variation along the $x$-axis and $y$-axis. Refer to equations (3-11) and (3-12) and figure 3-21. For a change along the $x$-axis, photocurrents going into sensor amplifiers $[1,1]$ $[1,2]$ $[3,1]$ $[3,2]$ $[2,3]$ $[2,4]$ $[4,3]$ and $[4,4]$ are varied from
0.1pA to 9.9pA while photocurrents going into sensor amplifiers [1,3] [1,4] [3,3] [3,4] [2,1] [2,2] [4,1] and [4,2] are varied from 9.9pA to 0.1pA.

Figure 3-23 Shows the node voltages at nodes for x-axis variation in photocurrents

For example if the photocurrent going into amplifier [1,1] is 3 pA then the photocurrent going into amplifier [3,3] will be 10pA-3pA = 7pA. Here we expect $V_{top}$ and $V_{bott}$ to have higher voltages than $V_{right}$ and $V_{left}$. Figure 3-23 shows that $V_{top}$ and $V_{bott}$ have higher voltages than $V_{right}$ and $V_{left}$ since there is little activity along the y-axis.

Similarly for a change along the y-axis photocurrents going into amplifiers [1,1] [1,3] [2,1] [2,3] [3,2] [3,4] [4,2] and [4,4] are varied from 0.1pA to 9.9pA while
photocurrents going into amplifiers [1,2] [1,4] [2,2] [2,4] [3,1] [3,3] [4,1] and [4,3] are varied from 9.9pA to 0.1pA. Here we expect \( V_{\text{right}} \) and \( V_{\text{left}} \) to have a higher voltage than \( V_{\text{top}} \) and \( V_{\text{bottom}} \).

![Graph showing node voltages at nodes for y-axis variation](image)

Figure 3-24 Shows the node voltages at nodes for y-axis variation

Figures 3-23 and 3-24 impress on us that variations along the x or y-axes relative to neighbors are converted into voltages, which are a function of the photocurrent. However a disturbing effect was that an increase in all the photocurrents means that the voltage at the nodes increases. This is undesirable. We need to locate the position of the spot independent of the absolute light intensity. Figure 3-25 shows what happens when we increase the current by a factor of two from 0.2pA to 19.8pA.
Figure 3-25 shows an undesirable effect for the variation along the $x$-axis. $V_{\text{bott}}$ and $V_{\text{top}}$ have a voltage jump of about 200mV due to an increase in the photocurrent. A large jump can also be observed for $V_{\text{right}}$ and $V_{\text{left}}$ for variations along the $y$-axis.

We need to incorporate normalization so that we are able to get rid of the increase in node voltage when the photocurrents all increase, i.e. make the phase computation independent of absolute light intensity.

3.4.1 Normalization

Further investigation into the matter led us to use a modified approach to address the issue of normalization, that is, keeping the centroid computation...
insensitive to light intensity. According to [Dav93] we can determine the $x$ and $y$ tilt of the wavefront averaged over the subaperture defined by the lenslet by using a difference between neighbors divided by the sum of all the photocurrents in a centroid. Using figure 3-10 (top left centroid) we may compute the first derivative of the phase in the $x$-direction using:

$$\frac{\partial u}{\partial x} = \frac{(I_{\text{photo}13} + I_{\text{photo}14}) - (I_{\text{photo}11} + I_{\text{photo}12})}{(I_{\text{photo}11} + I_{\text{photo}12} + I_{\text{photo}13} + I_{\text{photo}14})}$$  (3-19)

In our new approach, the second derivative along the $x$-axis is given by 3-20 while the second derivative along the $y$-axis is given by 3-21.

$$\frac{\partial^2 u}{\partial x^2} = \frac{(I_{\text{photo}11} + I_{\text{photo}12} + I_{\text{photo}23} + I_{\text{photo}24}) - (I_{\text{photo}13} + I_{\text{photo}14} + I_{\text{photo}21} + I_{\text{photo}22})}{(I_{\text{photo}11} + I_{\text{photo}12} + I_{\text{photo}13} + I_{\text{photo}14})} - \frac{(I_{\text{photo}11} + I_{\text{photo}12} + I_{\text{photo}23} + I_{\text{photo}24})}{(I_{\text{photo}13} + I_{\text{photo}14} + I_{\text{photo}21} + I_{\text{photo}22})}$$  (3-20)

$$\frac{\partial^2 u}{\partial y^2} = \frac{(I_{\text{photo}11} + I_{\text{photo}13} + I_{\text{photo}32} + I_{\text{photo}34}) - (I_{\text{photo}12} + I_{\text{photo}14} + I_{\text{photo}31} + I_{\text{photo}33})}{(I_{\text{photo}11} + I_{\text{photo}13} + I_{\text{photo}12} + I_{\text{photo}14})} - \frac{(I_{\text{photo}11} + I_{\text{photo}13} + I_{\text{photo}32} + I_{\text{photo}34})}{(I_{\text{photo}12} + I_{\text{photo}14} + I_{\text{photo}31} + I_{\text{photo}33})}$$  (3-21)

As equations 3-20 and 3-21 suggest the normalizing current is the sum of the currents going into each the sense amplifiers, we need to generate a copy of the photocurrent going into the sense amplifier so that we can feed it back to the summing node. This change effectively modifies our basic cell. Figure 3-25 shows the modification.
As in figure 3-16 all transistors have a $\frac{W}{L}$ ratio of $\frac{20}{6}$ while the cascode transistors have a $\frac{W}{L}$ ratio of $\frac{20}{3}$. As equations 3-20 and 3-21 suggest, photocurrents going into cell amplifiers have to be summed up. Transistors M24-M27 mirror the photocurrent going into the amplifier to generate $I_{ph_i}$. We then sum up all four photocurrents from neighboring current amplifiers in the centroid and inject them into M5 and M9 for each of the centroid amplifiers. This modification enables us to locate the position of the centroid independent of light intensity. One situation that we have to alleviate is a divide by zero; we externally inject an adjustable current of approximately 1pA at the 
summing point such that we always have a current going into M5 and M9 for each amplifier.

Of importance to us is that there should not be a big variation in the voltages at the nodes when we increase the input photocurrent. Now using a similar setup to the simulation that generated figure 3-25 we test the modified schematic that includes normalization. Results are shown in figure 3-27.

![Graph](image-url)

**Figure 3-27 Results from modified schematic (normalization)**

A comparison of results from figures 3-25 and 3-27 imply that the normalizing translinear amplifier is now insensitive to scaling in the input photocurrent.
Having determined that the circuit is now insensitive to increases in photocurrent we then proceed to simulate the transient nature of the cell amplifier. We want to make sure that it is stable for small and large changes in input photocurrent. Here we use $V_{DD} = +1.25$, $V_{SS} = -1.25$. A scaling current is fed into the drain of transistor M20 of figure 3-26. We input 31pA into the drain of M26 and connect this terminal to the drain of M9.

Next we input a current at node A. This current is stepped from 10pA to 11pA. Here we want to have a rough idea of the stability. Figure 3-28 shows the response to a step function.

The time it takes to reach 50% of the final value is the delay time, $\tau_d = 28.8\mu s$. The rise time, $\tau_r = 51.1\mu s$ is the time required to rise from 10% to 90% of the final value. Peak time $\tau_p$ is the amount of time required to reach peak overshoot and is equal to 104.8$\mu$s. Settling-time, $\tau_s$ is the time required for the response to reach and stay within 5% of the final value. It is 263.4$\mu$s. Figure 3-28 shows a response whose damping-factor $\zeta$, is slightly greater than one and thus is underdamped. Assuming a single time constant circuit, $f_{3db} = \frac{1}{2\pi\tau}$ and the rise time is $2.2\tau$. This approximation is handy since it is going to give us an approximation of the speed of the amplifier. A band width below 30khz is desired because that is the range for the biological retina. To simulate the results in figure 3-28 we used $V_{DD} = +1.25$
and \( V_{ss} = -1.25 \). Using the schematic of figure 3-26 we injected a photo current, \( I_{ph1} \), of 10pA, a scaling current \( I_{scaler} = 10nA \) and then we used a current of 40pA going into M9 to simulate the situation where all the other amplifiers are generating currents (normalization). This condition represents a case where the spot is located at the center of the centroid. Expected gain is computed below

\[
I_{outp} = I_{outn} = \frac{10 \text{pA} \times 10 \text{nA}}{40 \text{pA}} = 2.5 \text{nA}
\]  

(3-22)

Figure 3-28 Circuit response to a step function (10pA to 11pA).

From this approximation, we estimate the bandwidth of the amplifier to be 9.86kHz.

We also checked the response from a high to low step, from 11pA to 10pA. Results are shown in figure 3-29 and are similar to the stepped increase.
Figure 3-29 Circuit response to a step function (11pA to 10pA).

3.5 Circuit Implementation

3.5.1 Resistive grid

We proceed to replace the linear resistors with MOS devices. 50MΩ linear resistors are virtually impossible to integrate in a chip. MOS transistors operating in the ohmic region can emulate a 50MΩ resistor. They are linear for small voltage changes.

As was mentioned in chapter two, resistive grids achieve spatial smoothing; this enables us to perform local averaging. A signal injected into a resistive grid decays exponentially with distance from the source. If injected in the middle, the
effect spreads out in both directions. Node voltages are computed as was shown in chapter two. A one dimensional resistive grid resistive scheme is shown in figure 3-30. It is repeated from chapter two for convenience.

![Figure 3-30 Schematic of one a dimensional resistive grid (repeated)](image)

Nonlinear resistors are implemented using MOS devices connected in parallel. This configuration is compact since MOS devices do not occupy large silicon area. However, if a high sheet resistance layer is available such as lightly doped poly, it may be cost effective to use linear resistors.

NMOS and PMOS devices connected in parallel are operated in subthreshold. The small-signal channel resistance of a MOS transistor in strong inversion can be obtained using

\[
R_{ch}^{-1} = \frac{\partial I_{ds}}{\partial V_{ds}} \bigg|_{V_{gs}=\text{const}} = \frac{1}{k_n (V_{gs} - V_{th})} \tag{3-23}
\]

where \( k_n = KP \frac{W}{L} \).

Using the subthreshold saturation current equation, we may obtain an equation for the drain to source resistance of an MOS transistor operating in subthreshold [Omm99];
\[ I_{DS} = I_o \frac{W}{L} e^{\frac{V_{DS}}{V_T}} \left( e^{\frac{V_{DS}}{V_T} - \frac{V_{DS}}{V_T}} \right) \]  \quad (3-24)

When \( V_{DB} > V_{SB} + 5V_T \), the transistor is said to be in saturation

\[ I_{DS,\text{sat}} = I_o \frac{W}{L} e^{\frac{V_{DS}}{V_T}} \]

\[ R_{ch} = \left( \frac{\partial I_{DS}}{\partial V_{DS}} \right)^{-1} = \frac{I_o}{V_T} \frac{W}{L} e^{\frac{V_{DS}}{V_T}} e^{\frac{V_{DS}}{V_T}} \bigg|_{V_D=V_s} \]  \quad (3-25)

we may simplify (3-24) to

\[ R_{ch} = \frac{1}{I_{DS,\text{sat}}} \frac{1}{V_T} \]  \quad (3-26)

A schematic showing how we implemented resistors is shown in figure 3-31. \( I_b \), injected into the diode connected transistors sets the bias, so that MN and MP may operate as resistors in the ohmic region.

Figure 3-31 Pseudo-resistor [Omm99].
The drain and source terminals are interchangeable, hence current may flow in either direction.

For us to apply (3-25) we have to assume that the \( \frac{W}{L} \) ratios for all the devices are equal. To achieve a particular drain to source resistance we may vary this ratio or apply a particular bias current, \( I_b = I_{DS} \). Using \( V_T = 25\text{mV} \) and \( I_{DS} = 0.8\text{nA} \) we compute a resistance value of 31.25M\( \Omega \). This value is close to the simulated value in figure 3-32. This figure suggests that the pseudo-resistor is linear over a range of +/- 10mV; outside that range, the pseudo-resistance decreases. This is shown in figure 3-33. Here, the resistance has reduced to as low as 10M\( \Omega \).
3.5.2 Simulations using pseudoresistors

We then proceeded to hook up the entire system using pseudo resistors. For the ideal case we were using linear resistors. The value linear resistance between readout nodes is 100MΩ, so in order to get access to the injection node we use 50MΩ linear resistors on both sides. Pseudo resistors also need to be split into two, the setup shown in 3.5.1 will allow us to implement resistor value in the range 40MΩ, thus we have a resistance of 80MΩ between the readout nodes. Of course linear resistors will occupy a lot of silicon thus they are undesirable. Figure 3-3 shows an implantation of a two by two resistive grid using pseudo resistors.

Figure 3-32 CMOS Pseudo-resistor operating outside the linear region.
Figure 3-33 Two by two resistive grid using pseudoresistors.

Now replacing ideal resistors with MOS transistors and biasing them as was discussed in section 3.4.1. We need 50MΩ for each pseudo resistor. Using equation (3-25)

\[
R = \frac{V_T}{I_{DSres}}
\]  

We may compute \( I_{DSres} = 500\text{pA} \). With a supply voltage \( V_{DD} = +1.25\text{V} \) and \( V_{SS} = -1.25\text{V} \) we proceed to simulate a two by two resistive grid.

For a change along the \( x-axis \), photocurrents going into sensor amplifiers [1,1] [1,2] [3,1] [3,2] [2,3] [2,4] [4,3] and [4,4] are varied from 0.1pA to 9.9pA while
photocurrents going into sensor amplifiers [1,3] [1,4] [3,3] [3,4] [2,1] [2,2] [4,1] and [4,2] are varied from 9.9pA to 0.1pA.

Figure 3-34 Simulated node voltages for x-axis variation of a 2X2 phase reconstructor using pseudo-resistor

We also increase the intensity of the incoming current to see what effect it will have on the overall behavior of the circuit. This is a test for normalization; an increase in photocurrent should have no effect on the node voltage. Figure 3-35 shows that an increase in photocurrent has a small effect on the overall output. The change for $V_{\text{top}}$ and $V_{\text{bot}}$ is small, 2.67mV. However, there is an attenuation in all of the node voltage when pseudo-resistors are substituted for linear resistors. For instance, the
maximum voltage using the linear resistors was 1.21V in figure 3-27 while for figure 3-36 we are at 150mV. We may attribute this attenuation to the fact that the resistive value given by pseudo-resistors reduces below the nominal value once we operate outside of the voltage range of +/-10mV.

Figure 3-35 Simulated node voltages for y-axis variation of a 2X2 phase reconstructor using pseudo-resistor

Similarly for a change along the y-axis, photocurrents going into sensor amplifiers [1,1] [1,3] [2,1] [2,3] [3,2] [3,4] [4,2] and [4,4] are varied from 0.1pA to 9.9pA while photocurrents going into sensor amplifiers [1,2] [1,4] [2,2] [2,4] [3,1] [3,3] [4,1] and [4,3] are varied from 9.9pA to 0.1pA. Here we expect $V_{right}$ and $V_{left}$ to
have a higher voltage than $V_{\text{top}}$ and $V_{\text{bott}}$. We also increase the total intensity of the incoming currents to see what effect it will have on the overall behavior of the circuit. This is a test for normalization; an increase in photocurrent should have no effect on the node voltage. Results for this test are also incorporated. In figure 3-36 we have increased the photo current by a factor of two from 0.2pA to 19.8pA and the node voltages change by only 3.06mV at the extremes, which represents a 2% change. This shows that the configuration exhibits normalization. A change in photo current intensity does not affect our ability to compute the phase of the incident light.

Next we simulate the three by three-resistive grid configuration of figure 3-37. For this simulation we should note that we have a huge number of devices, 1344. Here for the $x$-axis variations, currents going into photo cells \([1,1,1] [1,1,2] [1,2,1] [1,2,2] [1,3,1] [1,3,2] [2,1,3] [2,1,4] [2,2,3] [2,2,4] [2,3,3] [2,3,4] [3,1,1] [3,1,2] [3,2,1] [3,2,2] [3,3,1] [3,3,2]\) are varied in the same direction while photocurrents going into photo cells \([1,1,3] [1,1,4] [1,2,3] [1,2,4] [1,3,3] [1,3,4] [2,1,1] [2,1,2] [2,2,1] [2,2,2] [2,3,1] [2,3,2] [3,1,1] [3,1,2] [3,2,1] [3,2,2] [3,3,1] [3,3,2]\) are varied in the opposite direction. We expect the voltage at $V_1$ to equal to the voltage at $V_3$ while the voltage at $V_2$ and $V_4$ will be the same but inverted to that of $V_1$ and $V_3$. Further when we increase the total input photocurrents we do not expect these voltages to change at all.
Figure 3-36 Three by three resistive grid.

Results for this simulation are shown in figure 3-38. Further, to show that normalization has been achieved we have increased the current to 19.8 pA for comparison. From figure 3-38 we may note that nodal voltages do not change with an increase in total photocurrent. In figure 3-38 $V_3$ and $V_4$ voltages have been offset by 2.5mV for clarity. Maximum output voltage varies from –150 mV to 150 mV.
Figure 3-37 Simulated voltages for the three-by-three pseudo-resistive grid in response to $x$-axis variations in the input photocurrents

Now for the $y$-axis variations, currents going into photo cells [1,1,1] [1,1,3] [2,1,1] [2,1,3] [3,1,1] [3,1,3] [1,2,2] [1,2,4] [2,2,2] [2,2,4] [3,2,2] [3,2,4] [1,3,1] [1,3,3] [2,3,1] [2,3,3] [3,3,1] [3,3,3] are varied in the same direction while photocurrents going into photo cells [1,1,2] [1,1,4] [2,1,2] [2,1,4] [3,1,2] [3,1,4] [1,2,1] [1,2,3] [2,2,1] [2,2,3] [3,2,1] [3,2,3] [1,3,2] [1,3,4] [2,3,2] [2,3,4] [3,3,2] [3,3,4] are varied in the opposite direction.

Results for this simulation are shown in figure 3-39. To further to show that normalization has been achieved we have increased the current to 19.8 pA for comparison. From figure 3-39 we may also note that nodal voltages do not change.
with an increase in photocurrent. Further $V_1$ and $V_2$ voltages have been offset by 2.5mV for clarity.

Figure 3-38 Simulated voltages for the three-by-three pseudo-resistive grid in response to y-axis variations in the input photocurrents

3.6 Conclusions

We have characterized two solutions to the problem, a voltage-mode and current-mode approach. Both of these approaches have shown promising results. The voltage-mode approach requires that we convert a current into a voltage.

In this thesis we have chosen to operate in the current mode, in which no current–to-voltage conversion is done. Results obtained in figures 3-38 and 3-39
imply normalization of the amplified current with respect to the absolute light intensity. Further current mode operation provides circuit simplicity, higher operating speed, low power dissipation and higher dynamic range. For these reasons we chose to use the current amplifier approach.

In the next chapter we will address hardware testing and layout. For devices in subthreshold, matching is critical. In the layout we will apply layout-matching techniques so that we may alleviate the etching effect. A compact layout will mean better matching of devices; we therefore seek to make a basic cell that will be compact and proceed to lay out this basic cell as close to its neighbor as possible.
4 HARDWARE TESTING AND LAYOUT

Simulation results in section 3.2.2 do not agree very well with theory. Therefore, we measured the behavior of the basic cell in the laboratory. Experimental set up and procedure are shown in detail in appendix C.

4.1 Experimental Requirements

The currents that we are dealing with are small. They are in the order of MOS leakage currents typically 10’s of picoAmperes. We need to use a reliable method to measure these low currents. The measurement equipment should not interfere with the circuit function.

We set up the circuit inside an aluminum chip-testing box. We used batteries and a linear power supply inside the box for low noise. We also used an instrumentation amplifier to amplify signals in the box before taking measurements with test equipment. Instrumentation amplifiers are used in data acquisition whenever a small differential output must be accurately measured. An instrumentation amplifier must have high input impedance and a high common mode rejection ratio (CMRR). The structure shown in figure 4-1 is the ideal measurement option because theoretically it will draw zero current since inputs are MOS transistor gates and they show infinite input resistance. It also provides high CMRR and a precise dc gain that is adjustable by selecting different values for $R_1$ [Toum89]. The schematic of an instrumentation amplifier is shown in figure 4-1. The instrumentation amplifier gain is given by [Sedra98]
\[ V_0 = \left(1 + \frac{2R_2}{R_1}\right)(v_2 - v_1) \]  
(4-1)

Figure 4-1 Instrumentation amplifier [Sedra98]

We then proceeded to built two instrumentation amplifiers. Characterization and testing were done on both of them. Results are shown in figure 4-2. Both amplifiers show a gain of 20V/V. For clarity an offset of 20mV was added to instrumentation amplifier one. The LMC6482A dual operational amplifier was picked because it draws a very small amount of current into the input terminals, typically 20fA. We also used 1% error resistors to build the amplifier to ensure better matching and temperature stability. More details are given in appendix C. Results obtained in figure 4-2 imply that the instrumentation amplifiers built in the lab are adequate for taking measurements. The dc offset voltage measured was small; however, in every measurement that we took, we
compensated for the dc-offset by taking the difference between the measured result and the measured dc-offset.

Next, we had to generate very small currents. The idea is to use huge resistors to generate these currents. We needed to divide a voltage value to a level that would force a small amount of current through a large value resistor. An idea to help visualize the whole process is to consider the R2R ladder of figure 4-3. In general when input \( D_n \) is tied to \( V_{dd} \) and all the other inputs are grounded, the output voltage is given by [Bog97]

\[
V_o = \frac{V_{dd}}{2^{(N-n)}} \quad \text{for} \quad n = 0, 1, 2, ..., N-1
\]  

Figure 4-2 Instrumentation amplifier gain

where \( N \) is the number of binary inputs.
As an example, let us consider a four-bit R2R ladder where, \( N = 4 \) and \( n = 3 \)
that is, the most significant bit (MSB) is set to \( V_{DD} \) and all the other inputs are tied to
ground. Using equation 4-3 we compute that \( V_o = \frac{V_{DD}}{2} \) while the current across the
output resistor is given by \( I_o = \frac{V_{DD}}{4R} \).

![Figure 4-3 R2R ladder](image)

It follows then that to get the least current in a four-bit R2R setup we need to set
the least significant bit (LSB) to \( V_{DD} \) while all the other inputs are grounded. In this case
\( N = 4 \) while \( n = 0 \), and now using equation 4-3 we compute \( V_o = \frac{V_{DD}}{16} \) and \( I_o = \frac{V_{DD}}{32R} \).

4.2 Measurement Results

The schematic of figure 4-4 (repeated from chapter 3 for convenience) was then
built; we used an analog prototype chip fabricated using the 0.5-\( \mu \)m AMI \( n \)-well process
that I layed out, fabricated and tested. Details of the measurement setup are shown in
Appendix C. In the actual simulated cell we injected a photocurrent ranging from 0.1pA –
9.9pA(\( I_1 \)), a scaling current (\( I_2 \)) of 10nA and a normalizing current (\( I_3 \)) of 100pA.
Device sizes were picked to be 16\( \lambda \)/6\( \lambda \) in the simulation where \( \lambda = 0.3\mu \)m. Now using
$16\lambda/6\lambda$ and knowing that the device sizes on the digital prototype chip are $4000\ \lambda/15\ \lambda$ we obtain a scaling factor of 100. All currents are then scaled up by this factor to yield $I_1 = 1\text{nA}$, $I_3 = 10\text{nA}$ and $I_2 = 1\text{µA}$. The current ideal gain is computed by

$$I_4 = \frac{I_2 I_1}{I_3}$$

(4-3)

Based on figure 4-3 (R2R Ladder), we built the circuits of figure 4-5 to generate $1\text{nA}$, $10\text{nA}$ and $1\text{µA}$ respectively. Since we did not have a specific procedure to determine the current, we had to adjust the potentiometers to get the right current values. We then measured the current going into the diode-connected transistor and compared it to the current going out of the current mirror. This precaution was to confirm that the current mirror was working properly and to verify that leakage currents were not affecting the measured data. During actual measurement we included a $10\text{MΩ}$ at the output of the
1nA current mirror circuit. This is to allow us to measure the actual current going into the amplifier.

Figure 4-5 Current generation circuits (a) 1nA current, (b) 10nA current and (c) 1μA current.

We simulated and built the current generation circuits and measured the current flowing through specific resistors using the instrumentation amplifiers.
After ensuring that we had the correct amount of currents going into the current amplifier we measured output the current $I_4$. Results obtained from this experimental procedure are shown in figure 4-6. The measured data obtained in figure 4-6 appears to follow the simulated data more closely than the ideal curve. Simulated data was obtained using different spice models from 6 runs in the AMI-0.5µ C5N process at room temperature.

![Current Amplification Graph](image)

**Figure 4-6** Plot of output current versus input photo current

Since the analog chip was fabricated using run t06f we repeated our simulations using models from this run and plot the results in figure 4-7. It shows that the actual measured data may be split into two regions. Region A is a high gain region. This region
is characterized by a steep slope. In this region leakage currents are on the order of the photocurrents that we are injecting into the amplifier. Region B has reduced gain, very to ideal value. This implies that working in this region will give results that are concurrent with the translinear principle. This is true because as we increase the photocurrents, $\kappa$ could be changing as a function of $V_{SB}$.

In appendix B we predicted reduced gain, as shown in figure 4-7. Note that in region B, most of the actual data falls between the ideal curve and that predicted when non-constant $\kappa$ is considered.
We also plotted the gain versus the input current in order to determine the region where we can get the best performance; this is shown in figure 4-8.

![Diagram showing gain versus input current](image)

Figure 4-8 Plot of gain versus the input current for the actual data and for the data obtained from the simulator (run t06f).

Results in figure 4-7 and 4-8 confirm that indeed our basic cell is obeying the translinear principle [And96]. The linear region, defined for the input currents from 5nA to 20nA, correspond to input photo-currents scaled down by a factor of 100 to 50pA to 200pA. According to [Del96] photocurrents of 25pA are typical in office lighting conditions for all pixel that is 1000µm². Thus 50pA is indeed a plausible input photocurrent.
4.3 Cell Layout

The aim of a good layout is compactness to minimize area. Source/drain terminals are shared, global signals like $V_{DD}$ and $V_{SS}$ are passed through the cell and signals that have to be shared between cells are also made available at the edge of the cell. Etch guards are introduced by say, adding devices that are disabled in the layout.

Figure 4-9 shows layout of the translinear amplifier. This cell is 61.5µm by 55.2µm. The cascode mirror transistors share their drain and source so that we may save on area. In addition ,minimum width and minimum spacing rules are applied wherever it is possible.
4.4 Centroid Layout

The layout in figure 4-10 shows how the centroid circuit should be hooked up. The photodiodes are placed next to each other so that we may have a shared aperture. As seen above the layout is very compact that means matching and etch-guarding have been
achieved. Further we need to incorporate the resistive grid and the node read out. Figure 4-11 below shows how we have incorporated the resistive grid and a follower.

Figure 4-11 Layout for the centroid incorporating the resistive grid and a follower.

The proposed chip floor plan is shown on figure 4-12. Here we have an 8X8 configuration. It is compact, thus here we will eliminate etching during fabrication.
Figure 4-12 Proposed chip floor plan 8X8 resistive grid

4.5 Layout versus schematic (LVS)

An LVS was conducted on each cell; it confirmed that the circuits are equal. LVS verifies that the schematic and the layout are equal. However, we had automorphed node classes. These are nodes which cannot be distinguished from one another by the LVS tool.
5 CONCLUSIONS AND RECOMMENDATIONS

5.1 Conclusions

This work has dealt with phase reconstruction based on centroid location; we have analyzed a technique that may be very useful in adaptive optics systems. The motivation behind this project was to come up with a single chip solution that will reconstruct the phase of a plane wave incident upon a surface. The entire work is based on the work previously published work of Furth and Clark [Fur98].

In chapter 3 we described the operation of the circuit. As we progressed through the material, it became apparent that intensity variations may modify our cell output. We employed normalization to ensure that our centroid computation is independent of absolute light intensity. Here we divide the output by the sum of the inputs to all the cells in the quadrant.

We have also described a second approach to the problem, a voltage-mode approach. Though this approach is straightforward, it showed a disadvantage due to its numerous current-to-voltage conversions.

In the current amplifier solution lenslets focus the phase orientation onto a spot and our centroid circuit should be able to determine the position of the focused spot. Signals from the centroid circuit are then injected into a resistive grid, which does phase reconstruction by giving a solution to Poisson’s equation. Further, in chapter 3 simulations are done to verify operation at the cell level. Based on the work by Meitzler [Meit93] we expect the circuit simulator not to converge for large dimensional systems. We therefore
performed simulations for a two by two-resistive grid and hooked up the whole system, predicting that the system is going to conform to theory. We also did a simulation for a three by three-resistive grid. We should note that in this case we are simulating of approximately 1400 devices. Layout versus schematic (LVS) verification was also done on cell level and on a two by two-resistive grid; it is unlikely that we will be able to perform an LVS on the entire design.

Compared to digital signal processing, analog signal processing is proving to be the way forward in large-scale neural computation. Analog processing has higher possible bandwidth and, given that the MOS devices operate in the subthreshold region, power consumption is extremely low. Further, sensory data is in the analog domain and thus compatibility to higher-level analog signal processing blocks is guaranteed. There is no need for costly A/D conversions. Further current mode operation provides circuit simplicity, higher operating speed, low power dissipation and dynamic range capabilities. Finally, low power circuits implemented in subthreshold occupy small silicon area, thus leading to higher yield.

The main problem that plagues circuits designed to operate in the subthreshold region is matching. Since the drain current is exponentially related to the gate to source voltage, any mismatch in these voltages can cause significant differences in the drain current [Bak98]. In subthreshold operation matching is critical. Matching implies two similar devices that show a constant ratio. A low matching ratio is ideal. Having this in mind we chose to pursue a compact layout that will have similar devices throughout the grid. A compact layout implies having devices as close as possible and ensuring that each
cell basically sees similar neighbors on all sides. As the layout shows, devices have been laid out as closely as possible to ensure good matching.

5.2 Recommendations

Testability is a major requirement in the VLSI process. We are at a disadvantage since we are yet to be able to make tests for this kind of chip. However VLSI and optical engineers should cooperate to come up with a complete system that should be able to incorporate my chip. The block diagram of figure 5-1 shows the entire setting. As the block diagram suggests we currently do not have the capability to construct a reliable method for testing this photo detector chip in our VLSI lab, however, its applications are numerous.

This work will be complete once we are able to read out the voltages at the nodes from the resistive grid. With this in mind, we need to be able to define the boundary conditions. We also need to come up with row, column decoders and buffers so as to enable testability of the chip. Further, students may be encouraged to pursue the differential voltage-mode approach so that they may quantify the pros and cons for voltage-mode versus current-mode approaches. Ideally integrating the photo detector, PDE solver and voltage to phase conversion in one chip will make the system very compact.
Figure 5-1 Block diagram incorporating the photodetector and PDE solver chip [Cla00]
APPENDICES
A. MODEL PARAMETERS AND SPICE LISTINGS

A.1 Model Parameters and SPICE listings

N-type Metal Oxide Semiconductor (NMOS) and P-type Metal Oxide Semiconductor (PMOS) models are obtained from MOSIS at this web address <http://www.mosis.org/cgi-bin/cgiwrap/umosis/swp/params/ami-c5n/t09w-params.txt>

A.1.1 NMOS Model

.model nmos nmos ( level = 49
+version = 3.1   tnom = 27   tox = 1.4e-8
+xj = 1.5e-7   nch = 1.7e17   vth0 = 0.6586834
+k1 = 0.9091227   k2 = -0.1093188   k3 = 23.8758374
+k3b = -9.7893829   w0 = 1e-8   nlx = 1e-9
+dvt0w = 0   dvt1w = 0   dvt2w = 0
+dvt0 = 3.2974199   dvt1 = 0.4121845   dvt2 = -0.0878853
+u0 = 463.5075226   ua = 2.635877e-11   ub = 1.577616e-18
+uc = 7.898745e-12   vsat = 1.472198e5   a0 = 0.5180082
+ags = 0.1243959   b0 = 2.974949e-6   b1 = 5e-6
+keta = -8.276092e-4   a1 = 0   a2 = 0.4277361
+rdsw = 1.566342e3   prwg = 0.0171695   prwb = 0.0202076
+wr = 1   wint = 3.036171e-7   lint = 3.430396e-8
+xl = 0   xw = 0   dwg = -2.777917e-8
+dwb = 3.020332e-8   voff = -0.0134897   nfactor = 0.8184494
+cit = 0   cdsc  = 2.4e-4   cdscd = 0
+cdscb = 0   eta0  = 0.0122481  etab  = -1.930584e-3
+dsusb = 0.2453226  pclm  = 2.274051  pdblc1 = -0.3210371
+pdlbc2 = 2.687653e-3  pdblcb = -0.0201843  drout  = 0.5957186
+pscbe1 = 5.324187e8  pscbe2 = 2.80409e-5  pvag  = 0
+delta = 0.01   rsh  = 80.4   mobmod = 1
+prt  = 0   ute  = -1.5   kt1  = -0.11
+kt1l = 0   kt2  = 0.022  ua1  = 4.31e-9
+ubl = -7.61e-18  uc1  = -5.6e-11   at = 3.3e4
+wl = 0  wln = 1  ww = 0
+wln = 1  wwl = -6.554e-20  ll = 0
+lIn = 1  lw = 0  lwn = 1
+lwl = -9.461e-20  capmod = 2  xpart = 0.4
+cgdo = 2.06e-10  cgso = 2.06e-10  cgbo = 1e-9
+cf = 4.237159e-4  pb = 0.9764175  mj = 0.4409532
+cjsw = 3.705201e-10  pbsw = 0.1  mjsw = 0.1212867
+pk2 = -0.0221848  wketa = -0.0246488  lketa = 2.463611e-3)

A.1.2  PMOS Model
.model pmos pmos ( level = 49
+version = 3.1  tnom = 27  tox = 1.4e-8
+xj = 1.5e-7    nch = 1.7e17    vth0 = -0.9728505
+k1 = 0.5231383  k2 = 0.0138873  k3 = 2.3151699
+k3b = -1.2633057  w0 = 1e-8    nlx = 1e-9
+dvt0w = 0    dvt1w = 0    dvt2w = 0
+dvt0 = 2.1708874  dvt1 = 0.4998361  dvt2 = -0.1097543
+u0 = 263.3045852  ua = 4.185433e-9  ub = 1e-21
+uc = -5.26721e-11  vsat = 2e5    a0 = 0.9022359
+ags = 0.1669013  b0 = 1.350109e-6  b1 = 5e-6
+keta = -2.185093e-3  a1 = 0    a2 = 0.3
+rdsw = 3e3  prwg = -0.0576125  prwb = -0.0504772
+wr = 1    wint = 3.728757e-7  lint = 2.816612e-8
+xl = 0    xw = 0    dwg = -4.479938e-8
+dwb = 4.986152e-9  voff = -0.0716981  nfactor = 0.9628956
+cit = 0  cdsc = 2.4e-4  cdscd = 0
+cdscb = 0  eta0 = 1.001219e-3  etab = 2.3485e-5
+dsub = 0.0464133  pclm = 2.212365  pdiblc1 = 0.0965102
+pdiblc2 = 2.484427e-3  pdibleb = -0.1  drout = 0.3071697
+pscbe1 = 5.105033e9  pscbe2 = 5.009248e-10  pvag = 0.3812043
+delta = 0.01  rsh = 102.1  mobmod = 1
+prt = 0  ute = -1.5  kt1 = -0.11
+kt1l = 0  kt2 = 0.022  ual = 4.31e-9
+ub1  =  -7.61e-18  uc1  =  -5.6e-11  at  =  3.3e4
+wl  =  0  wln  =  1  ww  =  0
+wln  =  1  wwl  =  -1.205e-20  ll  =  0
+lln  =  1  lw  =  0  lwn  =  1
+lwl  =  6.268e-21  capmod  =  2  xpart  =  0.4
+cgdo  =  2.27e-10  cgso  =  2.27e-10  cgbo  =  1e-9
+cj  =  7.302967e-4  pb  =  0.9535266  mj  =  0.4977403
+cjsw  =  2.650761e-10  pbsw  =  0.99  mjsw  =  0.2915271
+cf  =  0  pvth0  =  5.98016e-3  prdsw  =  14.8598424
+pk2  =  3.73981e-3  wketa  =  9.926074e-4  lketa  =  -3.394589e-3)
A.1.3 Current Amplifier Schematic

A.1.4 Spice Listing

* Main circuit: Activemodified

M2 Vdd vphoto Iphoto Vss NMOS W = 6u L = 1.8u AS = 9p AD = 9p PS = 15uPD = 15uM = 1

M3 Vdd vphoto N12 Vss NMOS W = 6u L = 1.8u AS = 9p AD = 9p PS = 15uPD = 15u

M1 N4 Iphoto Vss Vss NMOS W = 6u L = 1.8u AS = 9p AD = 9p PS = 15uPD = 15uM = 1
M7 N6 N12 Vss Vss NMOS W = 6u L = 1.8u AS = 9p AD = 9p PS = 15uPD = 15uM = 1

M8 N9 N12 Vss Vss NMOS W = 6u L = 1.8u AS = 9p AD = 9p PS = 15uPD = 15uM = 1

M12 N7 vcasc N6 Vss NMOS W = 6 L = 0.9u AS = 9p AD = 9p PS = 15uPD = 15uM = 1

M13 Ioutn1 vcasc N9 Vss NMOS W = 6 L = 0.9u AS = 9p AD = 9p PS = 15uPD = 15uM = 1

M4 vphoto vcasc N4 Vss NMOS W = 6 L = 0.9u AS = 9p AD = 9p PS = 15uPD = 15uM = 1

M5 N2 Iin Vss Vss NMOS W = 6u L = 1.8u AS = 9p AD = 9p PS = 15uPD = 15uM = 1

M6 N14 Iin Vss Vss NMOS W = 6u L = 1.8u AS = 9p AD = 9p PS = 15uPD = 15uM = 1

M14 Ioutn2 vcasc N13 Vss NMOS W = 6 L = 0.9u AS = 9p AD = 9p PS = 15uPD = 15uM = 1

M9 N13 N12 Vss Vss NMOS W = 6u L = 1.8u AS = 9p AD = 9p PS = 15uPD = 15uM = 1

M11 N12 vcasc N14 Vss NMOS W = 6 L = 0.9u AS = 9p AD = 9p PS = 15uPD = 15uM = 1
M10 Iin vcasc N2 Vss NMOS W = 6 L = 0.9u AS = 9p AD = 9p PS = 15uPD = 15uM = 1
M15 N8 Iscaler Vdd Vdd PMOS W = 6uL = 1.8u AS = 9pAD = 9pPS = 15uPD = 15uM = 1
M16 N11 Iscaler Vdd Vdd PMOS W = 6uL = 1.8u AS = 9pAD = 9pPS = 15uPD = 15uM = 1
M18 N3 N7 Vdd Vdd PMOS W = 6uL = 1.8u AS = 9pAD = 9pPS = 15uPD = 15uM = 1
M17 N10 N7 Vdd Vdd PMOS W = 6uL = 1.8u AS = 9pAD = 9pPS = 15uPD = 15uM = 1
M20 N7 vbiasp N10 Vdd PMOS W = 6 L = 0.9u AS = 9p AD = 9p PS = 15uPD = 15uM = 1
M21 Iscaler vbiasp N11 Vdd PMOS W = 6 L = 0.9u AS = 9p AD = 9p PS = 15uPD = 15uM = 1
M20 vphoto vbiasp N8 Vdd PMOS W = 6 L = 0.9u AS = 9p AD = 9p PS = 15uPD = 15uM = 1
M23 Ioutp1 vbiasp N3 Vdd PMOS W = 6 L = 0.9u AS = 9p AD = 9p PS = 15uPD = 15uM = 1
M19 N5 N7 Vdd Vdd PMOS W = 6uL = 1.8u AS = 9pAD = 9pPS = 15uPD = 15uM = 1
M24 Ioutp2 vbiasp N5 Vdd PMOS W = 6 L = 0.9u AS = 9p AD = 9p PS = 15uPD = 15uM = 1

* END OF MAIN CIRCUIT: ACTIVEMODIFIED.

* INPUT CIRCUIT FILE

.include G:\spring2001\Thesis\Tanner\T-Spice\Activemodified.sp

* SPICE MODELS

.include g:\spring2001\Thesis\Tanner\T-Spice\t09w05n.md
.include g:\spring2001\Thesis\Tanner\T-Spice\t09w05p.md

* IMPORTANT (DEFAULT) SIMULATION OPTIONS

.options abstol = 1e-018 chargetol = 1e-018 gmin = 1e-18 moscap = 1
.options relchargetol = 1e-15 reltol = 1e-15 vntol = 1e-15

* GRID SIZE AND RANGE FOR MOS I-V INTERNAL TABLES
* TO TURN OFF INTERNAL TABLES, SET DEFTABLES TO 0

.options deftables = 1

.vrange mos 5.5
.gridsize mos 128 256 64

* DC POWER SUPPLIES

VVdd Vdd Gnd 1.25
VVss Vss Gnd -1.25

* DC INPUTS (COMMENT OUT FOR LVS)

Ilphoto Iphoto Vss 10p
*Rscaler Iscaler Vss 160MEG

Ilscaler Iscaler Vss 10n

*Rin Vdd Iin 21000MEG

Ilin Vdd Iin 100p

*Current Sink

VVioutn1 Vdd ioutn1 0

VVioutn2 Vdd ioutn2 0

*Current Source

VVioutp1 Vss ioutp1 0

VVioutp2 Vss ioutp2 0

* Bias voltages

VVcasc Vcasc Vss 0.8

VVbiasp Vbiasp Vdd -1.1

*OUTPUT MEASUREMENT

.print dc i(VVioutn1)

.print dc i(VVioutn2)

*Current Source

.print dc i2(VVioutp1)

.print dc i2(VVioutp2)

*.print v(vphoto)

* Analysis
A.1.5 Modified current Amplifier Schematic

A.1.6 Spice listing

* Main circuit: Activemodified2

M2 N13 vphoto Iphoto Vss NMOS W = 6u L = 1.8uAS = 9pAD = 9pPS = 15uPD = 15uM = 1

M3 Vdd vphoto N1 Vss NMOS W = 6u L = 1.8uAS = 9pAD = 9pPS = 15uPD = 15uM = 1

M1 N5 Iphoto Vss Vss NMOS W = 6u L = 1.8uAS = 9pAD = 9pPS = 15uPD = 15uM = 1
M7 N10 N1 Vss Vss NMOS W = 6u L = 1.8u AS = 9p AD = 9p PS = 15u PD = 15u M = 1
M8 N6 N1 Vss Vss NMOS W = 6u L = 1.8u AS = 9p AD = 9p PS = 15u PD = 15u M = 1
M11 N1 Vcasc N2 Vss NMOS W = 6u L = 0.9n AS = 9p AD = 9p PS = 15u PD = 15u M = 1
M12 N9 Vcasc N10 Vss NMOS W = 6u L = 0.9n AS = 9p AD = 9p PS = 15u PD = 15u M = 1
M4 Vphoto Vcasc N5 Vss NMOS W = 6u L = 0.9n AS = 9p AD = 9p PS = 15u PD = 15u M = 1
M5 N8 Vnorm Vss Vss NMOS W = 6u L = 1.8u AS = 9p AD = 9p PS = 15u PD = 15u M = 1
M6 N2 Vnorm Vss Vss NMOS W = 6u L = 1.8u AS = 9p AD = 9p PS = 15u PD = 15u M = 1
M10 Vnorm Vcasc N8 Vss NMOS W = 6u L = 0.9n AS = 9p AD = 9p PS = 15u PD = 15u M = 1
M9 N3 N1 Vss Vss NMOS W = 6u L = 1.8u AS = 9p AD = 9p PS = 15u PD = 15u M = 1
M14 Ioutn2 Vcasc N3 Vss NMOS W = 6u L = 0.9n AS = 9p AD = 9p PS = 15u PD = 15u M = 1
M13 Ioutn1 vcase N6 Vss NMOS W = 6u L = 0.9nAS = 9pAD = 9pPS = 15uPD = 15uM = 1
M15 N7 I scaler Vdd Vdd PMOS W = 6uL = 1.8uAS = 9p AD = 9p PS = 15u PD = 15u M = 1
M16 N11 I scaler Vdd Vdd PMOS W = 6uL = 1.8uAS = 9p AD = 9p PS = 15u PD = 15u M = 1
M18 N12 N9 Vdd Vdd PMOS W = 6uL = 1.8uAS = 9p AD = 9p PS = 15u PD = 15u M = 1
M17 N15 N9 Vdd Vdd PMOS W = 6uL = 1.8uAS = 9p AD = 9p PS = 15u PD = 15u M = 1
M20 vphoto vbiasp N7 Vdd PMOS W = 6u L = 0.9nAS = 9pAD = 9pPS = 15uPD = 15uM = 1
M21 I scaler vbiasp N11 Vdd PMOS W = 6u L = 0.9nAS = 9pAD = 9pPS = 15uPD = 15uM = 1
M22 N9 vbiasp N15 Vdd PMOS W = 6u L = 0.9nAS = 9pAD = 9pPS = 15uPD = 15uM = 1
M23 Ioutp1 vbiasp N12 Vdd PMOS W = 6u L = 0.9nAS = 9pAD = 9pPS = 15uPD = 15uM = 1
M19 N14 N9 Vdd Vdd PMOS W = 6uL = 1.8uAS = 9p AD = 9p PS = 15u PD = 15u M = 1
M24 Ioutp2 vbiasp N14 Vdd PMOS W = 6u L = 0.9n AS = 9p AD = 9p PS = 15u PD = 15uM = 1

M32 N13 vbiasp N4 Vdd PMOS W = 6u L = 0.9n AS = 9p AD = 9p PS = 15u PD = 15uM = 1

M25 N4 N13 Vdd Vdd PMOS W = 6uL = 1.8uAS = 9p AD = 9p PS = 15u PD = 15u M = 1

M31 in vbiasp N16 Vdd PMOS W = 6u L = 0.9nAS = 9pAD = 9pPS = 15uPD = 15uM = 1

M26 N16 N13 Vdd Vdd PMOS W = 6uL = 1.8uAS = 9p AD = 9p PS = 15u PD = 15u M = 1

M28 N19 nonzero Vdd Vdd PMOS W = 3uL = 1.8uAS = 4.5p AD = 4.5p PS = 9uPD = 9uM = 1

M29 nonzero vbiasp N19 Vdd PMOS W = 3u L = 0.9nAS = 4.5pAD = 4.5pPS = 9uPD = 9uM = 1

M27 N18 nonzero Vdd Vdd PMOS W = 3uL = 1.8uAS = 4.5p AD = 4.5p PS = 9uPD = 9uM = 1

M30 in vbiasp N18 Vdd PMOS W = 3u L = 0.9nAS = 4.5pAD = 4.5pPS = 9uPD = 9uM = 1

* End of main circuit: Activemodified2
A.1.7  Pseudo Resistor Schematic

A.1.8  Spice listing

* Main circuit: PseudoR

M2 out Inn in Vss NMOS W = 3.6u L = 0.9u AS = 0.9u AD = 0.9u PS = 10.2u
PD = 10.2u M = 1

M1 Inn Inn Gnd Vss NMOS W = 3.6uL = 0.9u AS = 5.4pAD = 5.4pPS = 10.2u
PD = 10.2u M = 1

M3 out Inp in Vdd PMOS W = 3.6uL = 0.9u AS = 5.4pAD = 5.4pPS = 10.2u
PD = 10.2u M = 1

M4 Gnd Inp Inp Vdd PMOS W = 3.6uL = 0.9u AS = 5.4pAD = 5.4pPS = 10.2u
PD = 10.2u M = 1

* End of main circuit: PseudoR

.include G:spring2001\Thesis\Tanner\T-Spice\PseudoR.sp

* SPICE models

.include g:spring2001\Thesis\Tanner\T-Spice\t09w05n.md

.include g:spring2001\Thesis\Tanner\T-Spice\t09w05p.md

* Important (Default) Simulation Options
.options abstol = 1e-015 chargetol = 1e-015 gmin = 1e-15 moscap = 1
.options relchargetol = 1e-9 reltol = 1e-9 vntol = 1e-9

* Grid Size and Range for MOS I-V Internal Tables
* To turn off internal tables, set deftables to 0
.options deftables = 1

.vrange mos 5.5
.gridsize mos 128 256 64

* DC Power Supplies
VVdd Vdd Gnd 1.25V
VVss Vss Gnd -1.25v
VAgnd AGnd Gnd 0

* DC Inputs (Comment out for LVS)
VIout out Gnd 0
VVin in Gnd 0

* Loads (Comment out for LVS)
.dc VVIn -0.05 0.05 0.001

*II Vdd inn 0.8n
Rn Vdd inn 550Meg
*IInp inp Vss 0.8n
Rp inp Vss 250Meg

* Analysis
.options prtdel = 0.05n
.print dc i(Viout)

A.1.9 2x2 resistive grid (Using regular resistors)

A.1.10 Spice listing

.SUBCKT Activemodified2 in inorm Ioutn1 Ioutn2 Ioutp1 Ioutp2 Iphoto Iscaler
+ nonzero vbiasp(vcasc Vdd Vss
M2 N13 vphoto Iphoto Vss NMOS W = 6u L = 1.8uAS = 9pAD = 9pPS = 15uPD = 15uM = 1
M3 Vdd vphoto N1 Vss NMOS W = 6u L = 1.8uAS = 9pAD = 9pPS = 15uPD = 15uM = 1
M1 N5 Iphoto Vss Vss NMOS W = 6u L = 1.8uAS = 9pAD = 9pPS = 15uPD = 15uM = 1
M7 N10 N1 Vss Vss NMOS W = 6u L = 1.8uAS = 9pAD = 9pPS = 15uPD = 15uM = 1
M8 N6 N1 Vss Vss NMOS W = 6u L = 1.8uAS = 9pAD = 9pPS = 15uPD = 15uM = 1
M11 N1 vcasc N2 Vss NMOS W = 6u L = 0.9nAS = 9pAD = 9pPS = 15uPD = 15uM = 1
M12 N9 vcasc N10 Vss NMOS W = 6u L = 0.9nAS = 9pAD = 9pPS = 15uPD = 15uM = 1
M4 vphoto vcasc N5 Vss NMOS W = 6u L = 0.9nAS = 9pAD = 9pPS = 15uPD = 15uM = 1
M5 N8 inorm Vss Vss NMOS W = 6u L = 1.8uAS = 9pAD = 9pPS = 15uPD = 15uM = 1
M6 N2 inorm Vss Vss NMOS W = 6u L = 1.8uAS = 9pAD = 9pPS = 15uPD = 15uM = 1
M10 inorm vcasc N8 Vss NMOS W = 6u L = 0.9nAS = 9pAD = 9pPS = 15uPD = 15uM = 1
M9 N3 N1 Vss Vss NMOS W = 6u L = 1.8uAS = 9pAD = 9pPS = 15uPD = 15uM = 1
M14 Ioutn2 vcasc N3 Vss NMOS W = 6u L = 0.9nAS = 9pAD = 9pPS = 15uPD = 15uM = 1
M13 Iout1 vcase N6 Vss NMOS W = 6u L = 0.9nAS = 9pAD = 9pPS = 15uPD = 15uM = 1

M15 N7 Iscaler Vdd Vdd PMOS W = 6uL = 1.8uAS = 9p AD = 9p PS = 15u PD = 15u M = 1

M16 N11 Iscaler Vdd Vdd PMOS W = 6uL = 1.8uAS = 9p AD = 9p PS = 15u PD = 15u M = 1

M18 N12 N9 Vdd Vdd PMOS W = 6uL = 1.8uAS = 9p AD = 9p PS = 15u PD = 15u M = 1

M17 N15 N9 Vdd Vdd PMOS W = 6uL = 1.8uAS = 9p AD = 9p PS = 15u PD = 15u M = 1

M20 vphoto vbiasp N7 Vdd PMOS W = 6u L = 0.9nAS = 9pAD = 9pPS = 15uPD = 15uM = 1

M21 Iscaler vbiasp N11 Vdd PMOS W = 6u L = 0.9nAS = 9pAD = 9pPS = 15uPD = 15uM = 1

M22 N9 vbiasp N15 Vdd PMOS W = 6u L = 0.9nAS = 9pAD = 9pPS = 15uPD = 15uM = 1

M23 Ioutp1 vbiasp N12 Vdd PMOS W = 6u L = 0.9nAS = 9pAD = 9pPS = 15uPD = 15uM = 1

M19 N14 N9 Vdd Vdd PMOS W = 6uL = 1.8uAS = 9p AD = 9p PS = 15u PD = 15u M = 1
M24 Ioutp2 vbiasp N14 Vdd PMOS W = 6u L = 0.9nAS = 9pAD = 9pPS = 15uPD = 15uM = 1
M32 N13 vbiasp N4 Vdd PMOS W = 6u L = 0.9nAS = 9pAD = 9pPS = 15uPD = 15uM = 1
M25 N4 N13 Vdd Vdd PMOS W = 6uL = 1.8uAS = 9p AD = 9p PS = 15u PD = 15u M = 1
M31 in vbiasp N16 Vdd PMOS W = 6u L = 0.9nAS = 9pAD = 9pPS = 15uPD = 15uM = 1
M26 N16 N13 Vdd Vdd PMOS W = 6uL = 1.8uAS = 9p AD = 9p PS = 15u PD = 15u M = 1
M28 N19 nonzero Vdd Vdd PMOS W = 3uL = 1.8uAS = 4.5p AD = 4.5p PS = 9uPD = 9uM = 1
M29 nonzero vbiasp N19 Vdd PMOS W = 3u L = 0.9nAS = 4.5pAD = 4.5pPS = 9uPD = 9uM = 1
M27 N18 nonzero Vdd Vdd PMOS W = 3uL = 1.8uAS = 4.5p AD = 4.5p PS = 9uPD = 9uM = 1
M30 in vbiasp N18 Vdd PMOS W = 3u L = 0.9nAS = 4.5pAD = 4.5pPS = 9uPD = 9uM = 1

* End of main circuit: Activemodified2

.ENDS

.SUBCKT pixelinjmodified2 iphoto11 iphoto12 iphoto13 iphoto14 Iscaler nonzero
.+nx11 nx12 ny11 ny12 px11 px12 py11 py12 vbiasp vcasc Vdd Vss
XActivemodified2_1 isum isum nx11 ny12 px11 py12 iphoto11 I scaler nonzero vbiasp
+ vcasc Vdd Vss Activemodified2
XActivemodified2_2 isum isum nx12 ny12 px12 py12 iphoto13 I scaler nonzero vbiasp
+ vcasc Vdd Vss Activemodified2
XActivemodified2_3 isum isum nx11 ny11 px11 py11 iphoto12 I scaler nonzero vbiasp
+ vcasc Vdd Vss Activemodified2
XActivemodified2_4 isum isum nx12 ny11 px12 py11 iphoto14 I scaler nonzero vbiasp
+ vcasc Vdd Vss Activemodified2
.ENDS

* Main circuit: Currentinj2by2modified
Xpixelinjmodified2_1 Iphoto11 Iphoto12 Iphoto13 Iphoto14 I scaler nonzero N2 vtop
+ vleft N3 vtop N2 N3 vleft vbiasp vcasc Vdd Vss pixelinjmodified2
Xpixelinjmodified2_2 Iphoto31 Iphoto32 Iphoto33 Iphoto34 I scaler nonzero vtop
+ N86 vright N24 N86 vtop N24 vright vbiasp vcasc Vdd Vss pixelinjmodified2
Xpixelinjmodified2_3 Iphoto41 Iphoto42 Iphoto43 Iphoto44 I scaler nonzero vbot
+ N113 N110 vright N113 vbot vright N110 vbiasp vcasc Vdd Vss pixelinjmodified2
Xpixelinjmodified2_4 Iphoto21 Iphoto22 Iphoto23 Iphoto24 I scaler nonzero N66
+ vbot N94 vleft vbot N66 vleft N94 vbiasp vcasc Vdd Vss pixelinjmodified2

R1 node vtop 50Meg TC = 0.0, 0.0
R2 vtop Gnd 50Meg TC = 0.0, 0.0
R3 N3 Gnd 50Meg TC = 0.0, 0.0
R4 node vright 50Meg TC = 0.0, 0.0
R5 Gnd vright 50Meg TC = 0.0, 0.0
R6 Gnd N24 50Meg TC = 0.0, 0.0
R7 Gnd N86 50Meg TC = 0.0, 0.0
R8 N86 Gnd 50Meg TC = 0.0, 0.0
R9 N24 Gnd 50Meg TC = 0.0, 0.0
R10 Gnd N94 50Meg TC = 0.0, 0.0
R11 Gnd N94 50Meg TC = 0.0, 0.0
R12 Gnd N66 50Meg TC = 0.0, 0.0
R13 N66 Gnd 50Meg TC = 0.0, 0.0
R14 Gnd vbot 50Meg TC = 0.0, 0.0
R15 Gnd vleft 50Meg TC = 0.0, 0.0
R16 vbot node 50Meg TC = 0.0, 0.0
R17 Gnd N110 50Meg TC = 0.0, 0.0
R18 node vleft 50Meg TC = 0.0, 0.0
R19 Gnd N110 50Meg TC = 0.0, 0.0
R20 Gnd N113 50Meg TC = 0.0, 0.0
R21 N113 Gnd 50Meg TC = 0.0, 0.0
R22 Gnd N2 50Meg TC = 0.0, 0.0
R23 Gnd N3 50Meg TC = 0.0, 0.0
R24 N2 Gnd 50Meg TC = 0.0, 0.0

* End of main circuit: Currentinj2by2modified

* x-axis

* Input circuit file

.include G:\spring2001\Thesis\Tanner\T-Spice\currentinj2by2modified.sp

* SPICE models

.include g:\spring2001\Thesis\Tanner\T-Spice\t09w05n.md
.include g:\spring2001\Thesis\Tanner\T-Spice\t09w05p.md

* Important Simulation Options, here we are measuring very small values so these options have to be small

.options abstol = 1e-018 chargetol = 1e-018 gmin = 1e-18 moscap = 1
.options relchargetol = 1e-15 reltol = 1e-15 vntol = 1e-15

* Grid Size and Range for MOS I-V Internal Tables

* To turn off internal tables, set deftables to 0

.options deftables = 1
.vrange mos 5.5
.gridsize mos 128 256 64
* DC Power Supplies (slit supply)

VVdd Vdd Gnd 1.25

VVss Vss Gnd -1.25

VVcasc Vcasc Vss 0.8

VVbiasp Vbiasp Vdd -1.1

*DC Iphoto Currents

*the voltmeter is for measuring the current (cccs)

*Iphoto12 is dependant on Iphoto11

VVphoto11 Iphoto11 in1 0

IiIphoto11 in1 Vss 10p

fIphoto12 Iphoto12 Vss VVphoto11 1.0

fIphoto21 Iphoto21 Vss VVphoto11 1.0

fIphoto22 Iphoto22 Vss VVphoto11 1.0

fIphoto33 Iphoto33 Vss VVphoto11 1.0

fIphoto34 Iphoto34 Vss VVphoto11 1.0

fIphoto43 Iphoto43 Vss VVphoto11 1.0

fIphoto44 Iphoto44 Vss VVphoto11 1.0

*Iphoto13 is dependant on I4 and negative to Iphoto12

VVphoto31 Iphoto31 in3 0

fIphoto31 in3 Vss POLY(1) VVphoto11 10p -1

fIphoto32 Iphoto32 Vss VVphoto31 1.0
*scaling current 160nA

Rscaler Iscaler Vss 10Meg

*normalizing current 1.6nA

Isum nonzero Vss 16p

*Rsum nonzero Vss 24000Meg

*Output measurement

.print dc v(node)

.print dc v(vright)

.print dc v(vleft)

.print dc v(vbot)

.print dc v(vtop)

* Measurements

.dc llphoto11 0.1p 9.9p 0.1p

* A delay as I wait for results to settle

.options prtdel = 0.10n
.alter

flphoto31 in3 Vss POLY(1) VVphoto11 20p -1

.dc Ilphoto11 0.1p 19.9p 0.1p

y-axis

* Input circuit file

.include G:\spring2001\Thesis\Tanner\T-Spice\currentinj2by2modified.sp

* SPICE models

.include g:\spring2001\Thesis\Tanner\T-Spice\t09w05n.md
.include g:\spring2001\Thesis\Tanner\T-Spice\t09w05p.md

* Important Simulation Options, here we are measuring

* very small values so these options have to be small

.options abstol = 1e-018 chargetol = 1e-018 gmin = 1e-18 moscap = 1
.options relchargetol = 1e-15 reltol = 1e-15 vntol = 1e-15

* Grid Size and Range for MOS I-V Internal Tables

* To turn off internal tables, set deftables to 0

.options deftables = 1

.vrange mos 5.5
.gridsize mos 128 256 64

* DC Power Supplies (slit supply)

VVdd Vdd Gnd 1.25
VVss Vss Gnd -1.25
VVcasc Vcasc Vss 0.8
VVbiasp Vbiasp Vdd -1.1
VAgnd gnd Gnd 0

*DC Iphoto Currents

*the voltmeter is for measuring the current (cccs)

*Iphoto12 is dependant on Iphoto11

VVphoto11 Iphoto11 in1 0
IIphoto11 in1 Vss 10p
fIphoto12 Iphoto12 Vss VVphoto11 1.0
fIphoto21 Iphoto21 Vss VVphoto11 1.0
fIphoto22 Iphoto22 Vss VVphoto11 1.0
fIphoto33 Iphoto33 Vss VVphoto11 1.0
fIphoto34 Iphoto34 Vss VVphoto11 1.0
fIphoto43 Iphoto43 Vss VVphoto11 1.0
fIphoto44 Iphoto44 Vss VVphoto11 1.0

*Iphoto13 is dependant on I4 and negative to Iphoto12

VVphoto31 Iphoto31 in3 0
fIphoto31 in3 Vss POLY(1) VVphoto11 10p -1
fIphoto32 Iphoto32 Vss VVphoto31 1.0
fIphoto41 Iphoto41 Vss VVphoto31 1.0
flphoto42 Iphoto42 Vss V^Vphoto31 1.0
flphoto13 Iphoto13 Vss V^Vphoto31 1.0
flphoto14 Iphoto14 Vss V^Vphoto31 1.0
flphoto23 Iphoto23 Vss V^Vphoto31 1.0
flphoto24 Iphoto24 Vss V^Vphoto31 1.0

*scaling current 160nA
Rscaler Iscaler Vss 10Meg

*normalizing current 1.6nA

*Rin Vdd in 1320Meg

*ensure a non zero condition

*Rsum nonzero Vss 24000Meg

Isum nonzero Vss 16p

*Output measurement

.print dc v(node)

.print dc v(vright)

.print dc v(vleft)

.print dc v(vbot)

.print dc v(vtop)

* Analysis, dc sweep of the photocurrents
.dc IIphoto11 0.1p 9.9p 0.1p

* A delay as I wait for results to settle
.options prtdel = 0.1n

.alter

flip31 in3 Vss POLY(1) VVphoto11 20p -1

.dc IIphoto11 0.1p 19.9p 0.1p
B. EFFECT OF KAPPA

Results obtained in Figure 3-17 in chapter 3 do not agree well with theory. An analysis of the translinear loop on figure 3-13 is conducted below to ascertain why this is so. Loop $V_{SS} - A - B - C - V_{SS}$ yields

$$V_1 + V_2 = V_3 + V_4$$  \hspace{1cm} (B-1)

But knowing that the devices are in subthreshold the current through them in saturation is given by

$$I_D = S I_o e^{V_{GS}/V_T}$$  \hspace{1cm} (B-2)

Thus the gate to source voltage is given by

$$V_{GS} = \frac{V_T}{\kappa} \ln \left( \frac{I_D}{SI_o} \right)$$  \hspace{1cm} (B-3)

where $S = \frac{W}{L}$ and $\kappa_1 \neq \kappa_2 \neq \kappa_3 \neq \kappa_4$ due to body effect. $\kappa$ is a function of the bulk to source voltage. Using equation (B-3) we can rewrite (B-1) in the format shown below.

$$\kappa_T \left[ \frac{1}{\kappa_1} \ln \left( \frac{I_1}{SI_o} \right) + \frac{1}{\kappa_2} \ln \left( \frac{I_2}{SI_o} \right) - \frac{1}{\kappa_3} \ln \left( \frac{I_3}{SI_o} \right) - \frac{1}{\kappa_4} \ln \left( \frac{I_4}{SI_o} \right) \right] = 0$$  \hspace{1cm} (B-4)

$$\frac{1}{\kappa_1} \ln \left( \frac{I_1}{SI_o} \right) + \frac{1}{\kappa_2} \ln \left( \frac{I_2}{SI_o} \right) = \frac{1}{\kappa_3} \ln \left( \frac{I_3}{SI_o} \right) + \frac{1}{\kappa_4} \ln \left( \frac{I_4}{SI_o} \right)$$  \hspace{1cm} (B-5)

$$\ln \left( \frac{I_1}{SI_o} \right)^{\frac{1}{\kappa_1}} + \ln \left( \frac{I_2}{SI_o} \right)^{\frac{1}{\kappa_2}} = \ln \left( \frac{I_3}{SI_o} \right)^{\frac{1}{\kappa_3}} + \ln \left( \frac{I_4}{SI_o} \right)^{\frac{1}{\kappa_4}}$$  \hspace{1cm} (B-6)
Taking the inverse natural log

\[
\left( \frac{I_1}{S_{L_0}} \right)^{\frac{1}{\kappa_1}} \left( \frac{I_2}{S_{L_0}} \right)^{\frac{1}{\kappa_2}} = 1
\]

\[
\left( \frac{I_3}{S_{L_0}} \right)^{\frac{1}{\kappa_3}} \left( \frac{I_4}{S_{L_0}} \right)^{\frac{1}{\kappa_4}}
\]

\[
I_4^{\frac{1}{\kappa_4}} = \frac{\left( \frac{I_1}{S_{L_0}} \right)^{\frac{1}{\kappa_1}} \left( \frac{I_2}{S_{L_0}} \right)^{\frac{1}{\kappa_2}}}{\left( \frac{I_3}{S_{L_0}} \right)^{\frac{1}{\kappa_3}}} \cdot \frac{1}{(S_{L_0})^{\frac{1}{\kappa_4}}}
\]

\[
I_4 = \left( \frac{\left( \frac{I_1}{S_{L_0}} \right)^{\frac{1}{\kappa_1}} \left( \frac{I_2}{S_{L_0}} \right)^{\frac{1}{\kappa_2}}}{\left( \frac{I_3}{S_{L_0}} \right)^{\frac{1}{\kappa_3}}} \cdot \frac{1}{(S_{L_0})^{\frac{1}{\kappa_4}}} \right)^{\kappa_4}
\]

The above solution is valid for \( \kappa_1 \neq \kappa_2 \neq \kappa_3 \neq \kappa_4 \), since \( V_{SB} = 0 \) for M2 and M4 we may assume that \( \kappa_2 = \kappa_4 \) and \( \kappa_1, \kappa_3 > \kappa_2 = \kappa_4 \)

\[
I_4 = \left[ \frac{\left( \frac{1}{I_1^{\kappa_1}} \left( \frac{1}{I_2^{\kappa_2}} \right) \left( \frac{S_{L_0}}{I_3^{\kappa_3}} \right)^{\frac{1}{\kappa_3}} \right)^{\kappa_4}}{\left( \frac{1}{I_3^{\kappa_3}} \left( \frac{S_{L_0}}{I_3^{\kappa_3}} \right)^{\frac{1}{\kappa_3}} \right)^{\kappa_4}} \right]
\]

Equation (B-10) above should give us an idea of what to expect since simulations are giving us results that are contrary to the translinear principle [And96].
Now choosing $\kappa_2 = \kappa_4 = 0.7 \kappa_1 = 0.76 \kappa_3 = 0.75$, $S = \frac{W}{L} = \frac{20}{6} = 3.333$

and $I_o = 1$\textmu{}A we calculate $I_4 = 0.709$\textmu{}A.

$$I_4 = \left[ \frac{(3.4276) \times (3.72563) \times (50.349) \times 10^{-15} \times 10^{-12} \times 10^{-21}}{(46.7735) \times (161.674) \times 10^{-15} \times 10^{-21}} \right]^{0.7}$$

This computation suggests an attenuation, this is reasonable since $\kappa$ should in effect reduce the gain of our amplifier. This is a 28% reduction in value.

However using the equation below

$$I_{DS} = I_o \frac{W}{L} e^{\frac{\kappa V_{GB}}{V_T}} \left( e^{\frac{V_{GB}}{V_T}} - e^{\frac{V_{DS}}{V_T}} \right)$$ \hspace{1cm} (B-11)

For $V_{DS} > 4V_T$,

$$I_{DS} = I_o \frac{W}{L} e^{\frac{\kappa V_{GB}}{V_T}} e^{\frac{V_{GB}}{V_T}}$$ \hspace{1cm} (B-12)

$$I_{DS} = I_o \frac{W}{L} e^{\frac{\kappa V_{GB} - V_{GS}}{V_T}} = I_o \frac{W}{L} e^{\frac{\kappa V_{DS}}{V_T} - (1-\kappa)V_{GS}}$$ \hspace{1cm} (B-13)

We need to use equation B-13 to determine the effect of $\kappa$ satisfactorily.
C. HARDWARE TESTING

C.1 Current mode amplifier

Results obtained in chapter three do not follow the translinear principle [And96]. This uncertainty led us to take the schematic of figure 3-14 into the laboratory. Using a chip that was fabricated in 0.5-µm AMI n-well process we built and took measurements in order to determine the accuracy of the current mode amplifier.

C.2 Equipment and apparatus

1. Power supply (digital)
2. DMM (digital multimeter)
3. Chip testing box with breadboard and battery operated power supply.
4. Analog-0.5 µm AMI n-well process chip containing NMOS and PMOS current mirrors differential pairs and current conveyors.
5. LMC6482A (x4), 10kΩ+/−1%(x10), 100k+/−1%(x4), many regular 1MEG and 10 MEGΩ resistors

C.3 Experimental Setup

Here we describe a procedure for testing the current-mode-amplifier. We should note that we are working in subthreshold region and thus the currents are very small. However, we need to find a scaling ratio so that we may have a one-to-one comparison between our actual cell circuit and the built circuit.
The schematic for the current-mode-amplifier circuit is shown figure C-1. The output current is given by [And96]

\[ I_4 = \frac{I_2 I_1}{I_3} \]  

(C-1)

In the actual simulated cell we injected a photo current ranging from 0.1pA – 9.9pA(\(I_1\)), we also used a scaling current (\(I_2\)) of 10nA and a normalizing current (\(I_3\)) of 100pA. Device sizes were picked to be 16\(\lambda/6\lambda\).

![Figure C-1 Current mode amplifier circuit (repeated)](image)

Now using 16\(\lambda/6\lambda\) and knowing that the device sizes on the analog prototype chip are 4000\(\lambda/15\lambda\) we obtain a scaling factor of 100. All currents are then scaled up by this factor to give a normalizing current \(I_3\) of 10nA, a scaling current, \(I_2\) of 1\(\mu\)A and an input photocurrent ranging from 1nA to 25nA.
Small currents are measured using an instrumentation amplifier (figure 4-1). We are going to build the instrumentation amplifier using discrete operational amplifiers. We picked on the LMC6482A<http://www.national.com/pf/LM/LMC6482.html#Datasheet> because it has a very low input current of 20fA. The instrumentation amplifier ensures that we do not effect the circuit during measurements

C.4 Suggested Test Procedure

Split supply: Vdd = 1.5, Vss = -1.5V.

1. Build the instrumentation amplifiers; Use two LMC6482 to build one instrumentation amplifier. Hook pin8 and pin4 to Vdd and Vss respectively for both the two chips. On chip1 tie pin1 to pin2 through a 100K (+/-1%) resistor. Tie pin7 to pin6 through a 100kΩ (+/-1%) resistor. Tie pin2 to pin6 through a 10k (+/-1%) resistor. Note that your inputs to the instrumentation amplifier are pins3 and pins5 on the same chip. From pin1 tie attach a 10k (+/-1%) resistor and tie it to pin2 on the second ship. Also from pin7 tie attach a 10k (+/-1%) resistor to pin3 on the second chip. The output to the instrumentation amplifier is pin1. Tie pin1 to pin2 through a 10k(+/-1%) resistor. From Pin3 tie a 10k(+/-1%) resistor to analog ground. You have now built an instrumentation amp with a gain of 20. To check for the offset tie pins 3 and 5 on chip one together and measure the voltage output voltage from pin1 on chip two. What is the value? Next tie one of the inputs to ground and input a small dc input voltage to the other, measure the
output, from this calculate the instrumentation amp gain. Use small values say, from 1mv to 60 mV. Calculate the gain, comment. Next, build the second instrumentation amplifier and perform the same kind of tests, Note the gain and offset and comment on them. You have now built two instrumentation amplifiers that can be used to determine small values of currents through a resistor.

2. Only hook up Vdd (pin 20) and Vss (pin 40) to the PADS. Smell and touch chip to see if on fire.

3. Build the circuit of figure C-2 to generate 10nA. Determine the current going into the NMOS current mirror this is the normalizing current.

![Figure C-2 Schematic setup to generate 10nA](image)

4. Use figure C-3 to generate 1 µA.

![Figure C-3 Schematic setup to generate 1µA](image)
5. Build the circuit of figure C-4 to generate 1nA. Determine the current going into the NMOS current mirror. This is the simulated input photocurrent. You will need to vary this current by using a power supply ranging from 0 to 1.5 volts. Hook the negative lead to ground and vary the power supply voltage from 0 to 1.5V volts.

![Figure C-4 Schematic setup to generate 1nA](image)

6. Hook pin38 and pin 32 to Vdd, hook pin39 and pin31 to Vss. Tie pin29 to pin35. Tie pin30 to pin33. Sink a variable current (100pA to 1nA) through pin34. Source a stable current into pin 35 (1uA). Also sink a 10nA current through pin33. Hook a resistor (50K) to ground from pin28 (figure C-5) and determine the current through it using one of the instrumentation amplifiers. Tabulate the results. Vary the input voltage from 0.1 to 1.8V.

Notes:

a) The instrumentation amplifier is used to determine small voltage differences flowing through a resistor. We are using an instrumentation amplifier since it has a high input impedance and thus theoretically does not draw any current from the device being measured. Once we know this voltage we are then able to determine the current through the resistor since we know the resistor’s exact value.
b) Collect as much data as possible with fine points down in the 0.1nA-1nA range. Ensure that you also have a wide range of input photocurrents, say from 1-30nA.

c) Details of the analog prototype chip are in appendix D. Results obtained in figure 4-7 and 4-8 and are discussed in chapter four. With theoretical and experimental confirmation we are certain that the basic cell structure is going to work.

![Figure C-5 Wiring diagram](image)

Figure C-5 Wiring diagram
D. ANALOG PROTOTYPE CHIP

Project Name: Analog prototype chip (ajachip05)

Project Author: Alushulla Jacob Ambundo

Submitted: November 9, 1999

Fabrication: 0.5 µm AMI n-well process

Apparatus: Power Supply, DMM and a Chip Testing Box (breadboard)

Description: Requires a 40-pin chip that contains NMOS and PMOS current mirrors and current conveyors. Pin description is shown in table D-1 on the following page. The schematic for the chip is shown in figure D-1. All transistors are $W = 4000\lambda$ and $L = 15\lambda$ ($\lambda = 0.35\,\mu$m).
Table D-1 Pin description digital prototype chip

<table>
<thead>
<tr>
<th>Pin</th>
<th>Name</th>
<th>Pad Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Gate</td>
<td>Protect</td>
<td>Gate of PMOS Differential pair.</td>
</tr>
<tr>
<td>2</td>
<td>Gate</td>
<td>Protect</td>
<td>Gate of PMOS Differential pair.</td>
</tr>
<tr>
<td>3</td>
<td>Source</td>
<td>Bare</td>
<td>Source of PMOS Differential pair.</td>
</tr>
<tr>
<td>4</td>
<td>Drain</td>
<td>Bare</td>
<td>Drain of PMOS Differential pair.</td>
</tr>
<tr>
<td>5</td>
<td>Drain</td>
<td>Bare</td>
<td>Drain of PMOS Current Mirror.</td>
</tr>
<tr>
<td>6</td>
<td>Gate/Drain</td>
<td>Bare</td>
<td>Gate/Drain of PMOS Current Mirror.</td>
</tr>
<tr>
<td>7</td>
<td>Gate</td>
<td>Protect</td>
<td>Gate of a single PMOS transistor</td>
</tr>
<tr>
<td>8</td>
<td>Source</td>
<td>Bare</td>
<td>Source of single PMOS Transistor</td>
</tr>
<tr>
<td>9</td>
<td>Drain</td>
<td>Bare</td>
<td>Drain of single PMOS Transistor</td>
</tr>
<tr>
<td>10</td>
<td>Gate</td>
<td>Protect</td>
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Table D-1 (continued)
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Table D-1 (continued)
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Figure D-1 Schematic analog prototype chip
6  BIBLIOGRAPHY


