INTEGRATED CMOS OPTICAL PHASE SENSOR

BY

VAMSY PONNAPUREDDY, B.Tech.

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“INTEGRATED CMOS OPTICAL PHASE SENSOR,” a thesis prepared by
Vamsy Ponnapureddy in partial fulfillment of the requirements for the degree,
Master of Science in Electrical Engineering, has been approved and accepted by
the following:

_________________________________________________________________
Linda Lacey
Dean of the Graduate School

_________________________________________________________________
Paul Furth
Chair of the Examining Committee

_________________________________________________________________
Date

Committee in charge:

Dr. Paul Furth, Chair

Dr. David Voelz

Dr. Nancy Chanover
DEDICATION

Dedicated to God and my family.
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VITA

August 13, 1983  Born in Hyderabad, India.

August 2000- April 2004  B. Tech. in Electronics and Communication, Jawaharlal Nehru Technological University, India

Fall 2004-Spring 2005  Graduate assistant, Department of Geography, NMSU, Las Cruces, NM.

Fall 2006  Graduate teaching assistant, Klipsch School of Electrical Engineering, NMSU, Las Cruces, NM.

Field of Study

Major Field:  Electrical Engineering - VLSI Design
ABSTRACT

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Dr. Paul Furth, Chair

In many imaging applications, measurement of the phase of an optical wavefront is critical. This measurement is needed in applications such as optical surface profiling, non-destructive testing and adaptive optical correction. When a uniform optical wavefront is reflected by an optical surface or medium, there will be deviations in the phase of the wavefront due to the variations of the surface. Accurate measurement of the phase distribution across this wavefront gives an idea of the optical surface. A first generation CMOS sensor was previously developed at NMSU in order to detect the phase across an optical wavefront in real time. However, it did not function as expected because of a layout problem. In addition, in the first generation sensor, a binary counter was used as the reference clock.
This counter may cause problems with asynchronous sampling. In this thesis, a second generation sensor is developed that eliminates the problem of asynchronous sampling. Moreover, a novel technique of high-speed Gray-to-binary conversion is used. This sensor has an 8x8 array of pixels.

In addition, a novel method for testing the phase sensor was developed. In this method, two sinusoidal light signals with differing phases are used to form a light pattern. This pattern is focused onto the pixel array through a microscope and the relative phase between the two lights is estimated by the output difference between pixels. The correct function of this sensor is confirmed, as the digitized outputs of this sensor are close to the expected results.
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Chapter 1

INTRODUCTION

In many imaging applications, measurement of phase of an optical wavefront is critical. The motivation of this thesis is to design and test an integrated CMOS optical phase sensor for phase estimation of an optical wavefront. This sensor consists of an array of 8x8 pixels. The relative phase of the incoming optical wavefront across these pixels can be measured using this sensor. This sensor has many applications, such as optical surface profiling, non-destructive testing and adaptive optical correction.

In the subthreshold region of operation, MOS transistors consume very low power since the currents in this region are in the nanoampere to the picoampere range. Even the area required for systems designed in this region is very low. The analog portion of the integrated CMOS optical phase sensor was made efficient by using MOS transistors operating in subthreshold region.

The three major original contributions to this thesis are

- In this thesis, a new design of a high speed 8-bit Gray-to-Binary converter was implemented. In this new conversion technique, all the output bits are obtained almost simultaneously and the time required for conversion is also reduced to a large extent when compared to conventional conversion techniques. These advantages are achieved at the expense of more complex circuitry.
• This is the first time that this type of fully integrated sensor is working.

• A new method of testing was developed in this thesis using a setup in which two sinusoidal light signals, from sources such as LEDs, can be incident on the sensor to form a time-varying pattern. A microscope is used to focus the pattern on the sensor.

1.1 Overview

This thesis is organized as follows. In chapter 2, the complete background information is given, starting with a discussion of CCD and CMOS image sensors. We discuss the operation of the photodiode and modeling of the photodiode in CMOS. We also discuss the operation of the MOSFET in subthreshold region. Types of interferometric and phase measurement techniques are then discussed. Development of Binary-reflected Gray codes and their advantages over binary codes are also discussed.

In chapter 3, the architecture of the integrated CMOS optical phase sensor is explained. Different types of loads that can be used for the photodiode are mentioned and the results for the AC analysis of the photodiode with the load are shown. The implementation of a high pass filter using a capacitor and a transistor operating in the subthreshold region is explained. We also discuss the design of the comparator with hysteresis, static RAM cells and tri-state inverters. DC and transient analyses are then performed to verify the correctness of their operation. The design of the Gray code counter and decoder are explained. Then the design and simulation results of the novel Gray-to-Binary converter are discussed.

In chapter 4, the layouts of the circuits are shown. The setup used for optical testing is discussed. Then the measurement results of the sensor in both the electrical and optical environment are summarized.
In chapter 5, conclusions from the simulation and measurement results are discussed. Applications of this optical phase sensor are given. Finally, recommendations for future work are mentioned.
BACKGROUND INFORMATION

2.1 CCD and CMOS Image Sensors

Charge Coupled Device (CCD) and Complementary Metal Oxide Semiconductor (CMOS) image sensors are two different technologies for sampling images digitally. These imagers consist of several picture elements called pixels to store the light image information electronically at different locations.

In CCD imagers, the charge at each pixel in a row is transferred one after another to the readout register. After the charge of all the pixels in a row are transferred, the charge of pixels in the next row are transferred. From the readout register, the signal is fed to an output amplifier for charge-to-voltage conversion and then to an analog-to-digital converter. The digital output bits from the analog to digital converter are sent off the chip. Functions such as clock driving, timing generation and signal processing are normally kept on separate chips. So CCD cameras require a minimum of 3-4 different chips. In CCD imagers, the entire pixel is used for light capturing. So CCDs have 100% fill factor, which is defined as the percentage of the pixel that is devoted to collecting the light.

In CMOS imagers, each pixel has its own charge to voltage conversion. Many functions like timing generation, signal processing and analog-to-digital conversion are integrated together on the same chip. Additional features like anti-jitter and image compression can also be integrated on the chip at little extra cost. This on-chip integration makes CMOS cameras smaller, lighter and cheaper.
than a comparable CCD camera. As each pixel has some circuitry along with the photosensitive area for capturing light, the fill factor will not be 100% and this results in reduced sensitivity at low light levels.

Both imagers have their own advantages and disadvantages when compared to each other. CCDs have low noise, minimum non-uniformity, high sensitivity and a relatively simple fabrication process. CCDs have determined the performance benchmarks in photography in terms of image quality but at the expense of system size \[1\]. CCD imagers are also used in astronomical, aerospace, medical, graphic art and industrial applications. But the supply voltages are relatively large for CCD imagers.

CMOS imagers offer more integration, lower power dissipation and smaller system size when compared to CCD imagers. The size of CMOS pixels continues to decrease as CMOS technology becomes more advanced. Active-pixel architectures in CMOS consume much less power and allow integration of signal processing on chip. This is a great advantage in manufacturing video cell phones and compact camera systems.

2.2 Photodiode

A photodiode is a semiconductor diode that produces current in response to the incident optical power. It is used to detect optical power and to convert optical power into electrical power. A photodiode can be thought of as a light-controlled variable resistor. In complete darkness, it conducts little current as it has high resistance. When the photodiode is exposed to light, the resistance of the photodiode decreases and the current flow increases. Current produced by a photodiode is directly proportional to the light incident on it. As photodiodes respond quickly to changes in light intensity, they are extremely useful in digital
applications such as computer card readers, paper tape readers and photographic light meters. They are also used in some types of optical scanning equipment.

Photodiodes are fabricated from semiconductor materials like silicon or gallium arsenide. Silicon absorbs light over a characteristic wavelength of 250nm to 1100nm and gallium arsenide from 800nm to 2µm. The wavelengths of the light we can see range from 400nm-700nm. A photodiode is made of a $P – N$ junctions. $N$-type semiconductor material is doped with an excess of electrons and $P$-type semiconductor material has an excess of holes.

These holes and electrons experience a lower potential at the other end of junction. Due to this concentration gradient, holes diffuse into the $n$-layer and electrons diffuse into the $p$-layer. This movement establishes a depletion region, which has an electric field opposite and equal to the potential field created by the movement of charge. This depletion region is defined as the insulating region within a semiconductor material where there are no charge carriers. Due to this depletion region, no more current flows. A simple illustration of the depletion region formation in a $p – n$ junction is shown in Fig 2.1.

When photons of energy greater than the bandgap (1.1eV for silicon) of that material are absorbed by the crystal in the depletion region, electron-hole pairs are created. The electron-hole pairs drift apart and the electric field causes them to move. If the two sides of the junction are placed in a circuit, an external current flows through the junction.

Under no light conditions, when the photodiode is operated in reverse bias i.e., when the negative terminal of the battery is connected to the $p$-side of the junction and the positive terminal of the battery is connected to the $n$-side, the holes on the $p$-side and the electrons on the $n$-side move away from junction. Only small current called reverse saturation current flows through the photodiode.
This is also called dark current and it strongly depends on the temperature. If we illuminate a reverse-biased P-N junction, the number of new electron-hole pairs is proportional to the number of incident photons $[2]$. This mode of operation is called photoconductive mode.

Responsivity of a photodiode is defined as the ratio of photocurrent generated in Amperes to the incident light power in Watts. The silicon photodiode response is mostly linear from the minimum detectable light power up to several milliWatts. With an increase in the reverse bias voltage, the depletion region gets wider and the linearity and responsivity improves $[3]$. In reverse bias mode, photodiodes exhibit fast switching speeds.

**2.3 CMOS Phototransconduction using Photodiodes**

Photodiodes and phototransistors are the basic types of devices that can be used for photodetection in the standard CMOS process. These devices are
somewhat less efficient than the devices specially built for photodetection [4]. In the following sections, the properties of CMOS photodiodes are discussed.

In the standard CMOS process, the \textit{n}-type and \textit{p}-type layers are produced by an implantation mechanism and, hence, the borders are not sharp. Three possible photodiode devices that can be formed in CMOS are: the \textit{n+}/\textit{p}-substrate photodiode, the \textit{p+}/\textit{n}-well photodiode and the \textit{n}-well/\textit{p}-substrate photodiode. The first two are shallow junction photodiodes and the third photodiode is a deep junction photodiode [5]. The structures of these three photodiodes are shown in Fig 2.2.

**The \textit{n+}/\textit{p}-substrate Photodiode**

This is the most widely used photodiode in the conventional CMOS process. The junction formed is between \textit{n}-diffusion and a \textit{p}-substrate. The spectral range of this photodiode is better than that of \textit{p+}/\textit{n}-well photodiode [6]. It has a simple layout and is less susceptible to fixed pattern noise. But this diode is vulnerable to crosstalk and noise due to diffusion and leakage of carriers through the substrate. The maximum quantum efficiency occurs at a wavelength of 620nm. This diode has the lowest dark current when compared to the two other photodiodes.

**The \textit{p+}/\textit{n}-well Photodiode**

This photodiode is formed with \textit{p}-diffusion in an \textit{n}-well. The spectral response of this diode is more narrow when compared with other photodiodes. Due to the narrowness and shallowness of the \textit{p+}/\textit{n}-well junction, the spectral response is degraded. The \textit{n}-well/\textit{p}-substrate junction shields the charge carriers generated outside the \textit{n}-well and hence leads to lower crosstalk between neighboring photodiodes. The maximum quantum efficiency occurs at wavelength of 530nm (green). This photodiode has a faster response when compared with the other photodiodes. This diode has the worst dark current compared with other junction diodes.
The n-well/p-substrate Photodiode

This type of junction is formed between an n-well and the p-substrate. Due to the wideness and deepness of its depletion region, this photodiode has the best spectral response for visible light. This photodiode has the lowest capacitance, which helps to achieve a high bandwidth. The disadvantage of this diode is its
sensitivity to substrate noise and crosstalk from the neighboring photodiodes. This junction has moderate dark current compared with other junction diodes [5].

2.4 Modeling a CMOS Photodiode

The equivalent circuit of a photodiode is shown in Fig 2.3. $I_L$ is the current generated by the incident light, $I_D$ is the diode current, $C_J$ is the junction capacitance, $R_{SH}$ is the shunt resistance and $R_S$ is the series resistance.

![Photodiode equivalent circuit.](image)

When the photodiode is reverse-biased, it acts as the current source. For a CMOS photodiode, the shunt resistance is very high and the series resistance is very low. So, neglecting these resistances, the equivalent circuit is simply a junction capacitance in parallel to a current source which is proportional to the light incident on the photodiode. The equivalent model for a CMOS photodiode is shown in Fig 2.4. In circuit simulations, light sources and photodiodes can not be used. So this photodiode model is used instead of a reverse biased photodiode in simulations in Cadence.

A photodiode in CMOS is formed by placing an $n+$-diffusion in a $p$-substrate. The DC characteristics of the $n+$-diffusion/$p$-substrate $PN$ junction
diode is given as

\[ I_D = I_S \left( e^{\frac{V_d}{nUT}} - 1 \right) \]  (2.1)

where \( I_D \) is the diode current, \( I_S \) is the saturation current, \( V_d \) is the voltage across the diode, \( n \) is the emission coefficient and \( U_T \) is the thermal voltage which is given by

\[ U_t \equiv KT/q \]  (2.2)

where K is the Boltzmann’s constant, T is the temperature and q is the magnitude of electronic charge. Thermal voltage is approximately 26mV at room temperature.

The junction capacitance of a CMOS photodiode is given as

\[ C_{ph} = C_J.A + C_{JSW}.P \]  (2.3)
where \( C_J \) is the bottom plate junction capacitance per unit area, \( C_{JSW} \) is the sidewall junction capacitance per length, \( A \) is the bottom area and \( P \) is the sidewall perimeter of the \( n^+ \)-diffusion region.

### 2.5 Subthreshold Conduction

Generally it is assumed that the MOSFET turns off abruptly as \( V_{GS} \) drops below \( V_{TH} \). But in reality, a weak inversion layer exists for \( V_{GS} \approx V_{TH} \) and some current flows from drain to source \(^7\). When \( V_{GS} \) is below the threshold voltage and the MOSFET is in weak inversion, the current that flows from drain to source is called subthreshold current. In large circuits such as memories, even when the circuit is switched OFF the subthreshold conduction can result in significant power dissipation or loss of analog or digital information. This current exhibits an exponential dependence on \( V_{GS} \). The current through the “channel” in this region is dominated by diffusion of minority carriers and is given by \(^8\)

\[
I_D = I_0 \frac{W}{L} e^{\kappa V_{GB}/U_t} \left( e^{-\frac{V_{SB}}{U_t}} - e^{-\frac{V_{DB}}{U_t}} \right)
\]

where \( V_{GB} \) is the gate to bulk voltage, \( V_{SB} \) is the source to bulk voltage, \( V_{DB} \) is the drain to bulk voltage, \( W/L \) is the width to length ratio, \( I_0 \) is the zero-bias current, \( \kappa \) is the electrostatic coupling coefficient between the gate and “channel”, and \( U_t \) is the thermal voltage.

The exponential relation between \( V_{GS} \) and \( I_D \) is similar to that between \( V_{BE} \) and \( I_C \) relation in a bipolar transistor. This exponential relation is useful in translinear circuits. The drain current \( I_D \) in the subthreshold region is in the picoamperes to nanoamperes range.
From the equation for the drain current,

For \( V_{SB} = 0, V_{DS} = 0 \Rightarrow I_D = 0 \)

For \( V_{SB} = 0, V_{DS} = U_t \Rightarrow I_D = 0.63I_0 \frac{W}{L} e^{\kappa V_{GS}/U_t} \)

For \( V_{SB} = 0, V_{DS} = 2U_t \Rightarrow I_D = 0.86I_0 \frac{W}{L} e^{\kappa V_{GS}/U_t} \)

For \( V_{SB} = 0, V_{DS} = 3U_t \Rightarrow I_D = 0.95I_0 \frac{W}{L} e^{\kappa V_{GS}/U_t} \)

For \( V_{SB} = 0, V_{DS} = 4U_t \Rightarrow I_D = 0.98I_0 \frac{W}{L} e^{\kappa V_{GS}/U_t} \)

For \( V_{SB} = 0, V_{DS} > 4U_t \Rightarrow I_D \approx I_0 \frac{W}{L} e^{\kappa V_{GS}/U_t} \)

For \( V_{DS} \leq 4U_t \), the transistor will be in the ohmic region. For \( V_{DS} > 4U_t \approx 100mV \), it will be in the saturated subthreshold region. In the saturated subthreshold region, the transconductance \( g_m \) is given by

\[
g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{\kappa I_D}{U_t} \tag{2.5}
\]

The small signal resistance between drain and source in saturated subthreshold region is given by

\[
r_0 = \frac{V_A}{I_D} \tag{2.6}
\]

where \( I_D \) is the drain current and \( V_A \) is the early voltage, which has units of Volts. Since long devices are less affected by channel-length modulation, they have higher Early voltages. The Early voltage is directly proportional to the length of the device. Typical values of Early voltage range from 5V to 50V.

The exponential dependence of \( I_D \) upon \( V_{GS} \) in the saturated subthreshold operation may be useful in achieving higher gain by operating MOSFET devices in this regime. But the main drawback of operating devices in this regime is that the speed of the circuits is very low. In order to operate a device in subthreshold,
either it must be of large size or the drain current must be very low. If the drain currents are low, it takes a longer time to charge and discharge the output capacitance and thus the speed of the circuit is limited. One more disadvantage of operating in this regime is mismatch. As $I_D$ depends upon $V_{GS}$ exponentially, a small change in $V_{GS}$ results in a significant change in $I_D$. In circuits like current mirrors, a small difference in $V_{GS}$ leads to a significant mismatch in $I_D$ and thus it leads to large mismatch errors [9].

2.6 Comparators

A voltage comparator is a circuit that compares the instantaneous value of the input signal with the reference signal and produces a binary output depending on whether the input signal is greater or less than the reference signal. A comparator has two inputs, namely a non-inverting input and an inverting input and one output. If the signal at the non-inverting input is higher than the signal at the inverting input, then the output goes high. If the signal at the inverting input is higher than the signal at the non-inverting input, then the output goes low. Comparators are commonly used in analog to digital converters. They can be implemented using an op-amp with no internal compensation.

Propagation delay and sensitivity are important factors to be considered when designing a comparator. The propagation delay is defined as the time between the input voltage crossing the reference voltage and the output voltage switching its state. The propagation delay should be as low as possible. The sensitivity of a comparator is defined as the minimum voltage difference between the input and the reference signal that a comparator can detect.

Hysteresis is a useful property of a comparator where the output switches for two different input threshold values depending on whether the input is rising or falling. The difference between these two threshold values is defined as the
hysteresis of the comparator. A circuit will be less sensitive to noise when some amount of hysteresis is added to the circuit. As such we can get a clean output. By adding positive feedback to the circuit, we can introduce a small amount of hysteresis to the system. Comparators can be categorized as comparators with internal hysteresis and comparators with external hysteresis, depending on how the positive feedback is applied to the circuit [9].

2.7 Binary Reflected Gray Code

A Gray code is a way of encoding binary numbers so that adjacent numbers differ by only a single bit. There are large number of possible legitimate Gray codes. Out of these possibilities, one particular realization of the Gray code is very useful and very important. This is called the “binary reflected Gray code” or simply “The Gray code.” The name of the binary-reflected Gray code is derived from the fact that the second half of the values in this code are equivalent to the first half, in reverse order, except for the highest significant bit which is inverted. The Gray code was named after a Bell Labs researcher Frank Gray.

The Gray code is invented by a French engineer, Emile Baudot, in 1878. It was originally called “cyclic permuted code.” He used it in telegraphy. Later Frank Gray invented the method of converting the analog signals into Gray reflected binary codes. One advantage of this code is that in conversion of analog signals to digital output, the error is minimal. One important application of Gray codes is that it is used for error correction in digital communications. This code is closely related to the solution of the famous puzzle, towers of Hanoi.

In the Gray code, the first two numbers, zero and one, are represented by digits 0 and 1. The next two numbers, two and three, are represented by 11 and 10 as shown in Fig 2.5(a). A mirror represented by the dashed line is placed below the first half of the numbers, giving rise to the reflection (i.e., the same numbers
but in reverse order) [10]. Then the digit 0 is prepended to the numbers in the upper half above the mirror and the digit 1 is prepended to the numbers in the lower half below the mirror. So the numbers 0, 1, 2, 3 are represented by 00, 01, 11, 10, respectively, in the Gray code. For the next repetition, numbers 4, 5, 6, 7 are developed. Thus, successive repetitions allow us to extend the Gray code representation. The Gray codes for the first eight and sixteen numbers are shown in Fig 2.5(b,c). First half of the values in this code are equivalent to second half in the reverse order, except for highest significant bit is 0 for first half and 1 for second half.

Figure 2.5: Development of Binary Reflected Gray Code (a)2-bit (b)3-bit and (c)4-bit.
This method of generating the Gray code makes the useful property that successive numbers in the code differ by only one digit. For example, numbers 3 and 4 are represented in binary code as 011 and 100 respectively. These two successive codes differ by all three bits. But in the Gray code, numbers 3 and 4 are represented by codes 010 and 110 respectively. These codes differ by only one bit. As a single output bit changes at a time, this Gray code is used in asynchronous sampling circuits and permits asynchronous combinational circuits to operate independently. This Gray code also has potential for saving power.

One problem with standard binary codes is that, in real circuits, it is very unlikely that bits in the code switch states exactly at same time. For example, if the code value changes from 3(011) to 4(100), all the three code bits change state. From state 011 to 100, the transition of bits will not occur at exactly the same time. The transition might look like 011 - 010 - 110 - 100. When the code is in transition, say at 010, one cannot say if it at real state, or if it is at an intermediate state. If this code is fed to a sequential circuit, then this circuit may store a false value. But with Gray codes, there will not be any intermediate states as only one code bit changes between successive states. Thus Gray codes are useful in asynchronous sampling circuits.

The algorithm for converting between the binary-reflected Gray code and standard binary code is very simple. Assume that \( i^{th} \) bit of a binary code string is represented by \( B[i] \) and the \( i^{th} \) bit of Gray code string is represented by \( G[i] \). The most significant bit of both of the codes is the same. For other less significant bit, the equation for converting from binary to Gray code is \( G[i] = B[i+1] \ XOR B[i] \) and the equation for converting from Gray to binary code is \( B[i] = B[i + 1] \ XOR G[i] \).
2.8 Terms from Optics

2.8.1 Wavefront

A wavefront is defined as the locus of points having the same phase i.e., the same path length. Since optical frequencies are so high, the temporal component of the waves is usually ignored at these wavelengths and only the phase of the spatial oscillation is critical. Most detectors are indifferent to polarization, so even this property of the optical signal is usually ignored. At radio wavelengths (3kHz to 300GHz), detectors are usually phase-sensitive. Many audio detectors (15Hz to 20kHz) are also phase-sensitive. When an optical signal propagates through different temperature layers and different wind speeds, they get distorted. Using adaptive optics these kind of distortions can be corrected.

2.8.2 Interferometry

Interferometry is derived from the word interference. Interference is the superimposition of two or more waves resulting in a new wave pattern. Interference can be thought of as adding two waves with each other. Depending on the amplitude of the waves and the phase difference between the waves, the two waves will either add or cancel. This kind of interferences are called constructive interference and destructive interference, accordingly.

Interferometry is the use of this interference phenomenon for making measurements. An interferometer is the device for making measurements. These devices work on the basic principle that a beam of light from a single source is split into two or more beams using mirrors and then these beams are recombined so as to interfere with each other. This results in alternate bands of light and dark called fringes. When beams are added constructively, the fringes are bright and when the beams cancel out each other, the fringes are dark.
There are different types of interferometers though all of them work on the same basic principle. The most commonly used interferometers are the Michelson interferometer, the Mach-Zehnder interferometer, the Sagnac interferometer and the Fabry-Perot interferometer.

2.8.3 Beat Note

If two laser beams of different frequencies are superimposed on a photodetector, a signal with the difference of the two optical frequencies called beat note is observed [11]. To observe this beat note, the following conditions have to be met

- The optical frequency of the beat note must be within the bandwidth of the detector.
- The spatial distributions of the two superimposed light fields must not be orthogonal.
- The polarization states of the two beams must not be orthogonal.
- The wavelengths must be within the range where the photodetector is sensitive.

The beat note optical frequency output is generally measured using a frequency counter or a spectrum analyzer. In frequency measurement techniques, the frequency of one laser can be measured by recording a beat note between this laser and that of another laser of known frequency that is close to the first one. When an optical signal of frequency 80MHz is superimposed with an optical signal of frequency 80.01MHz on a detector, then a beat note of frequency 10kHz is observed.
2.9 Types of Interferometry

The basic operation is the same for all interferometers, where the light beam is split into two arms and are brought together and superimposed. Michelson interferometry and Mach-Zehnder interferometry are the two most commonly used interferometries and they are explained in this section.

2.9.1 Michelson Interferometry

The American physicist Albert Michelson invented the optical interferometer shown in Fig 2.6. This interferometer is constructed using a half-silvered mirror inclined at a $45^\circ$ angle to the incoming beam. The incoming beam is split into two beams of equal amplitude by this half-silvered mirror. One beam reflects off the half-silvered mirror to the fixed mirror, reflects back to the half-silvered mirror, then passes through the half-silvered mirror to the detector. The other beam goes through the half-silvered mirror to the movable mirror and reflects back to the half-silvered mirror and then reflects off the half-silvered mirror to the detector. These two sub-beams are superimposed to form an interference pattern.

The movable mirror can be moved by a very small distance. By moving this mirror, the path length of the corresponding sub-beam is changed and hence the phase relation between the two sub-beams. If the path lengths of the two sub-beams are $x_2$ and $x_1$, the optical path length difference is given by $\Delta x = x_2 - x_1$. A related quantity is the phase difference, $\Delta \phi$, given by

$$\Delta \phi = \frac{2\pi}{\lambda} \Delta x = \frac{2\pi}{\lambda} (x_2 - x_1) \quad (2.7)$$
Constructive interference occurs when

$$\Delta x = m\lambda \text{ (or) } \Delta \phi = 2m\pi, \text{ For } m = 0, \pm 1, \pm 2, \ldots \quad (2.8)$$

Destructive interference occurs when

$$\Delta x = \pm \frac{2m + 1}{2}\lambda \text{ (or) } \Delta \phi = \pm(2m + 1)\pi, \text{ m = 0, 1, 2, ...} \quad (2.9)$$

Figure 2.6: Michelson Interferometer.
The intensity of the interference pattern is given by

\[ I(x, y) = I_1 + I_2 + 2\sqrt{I_1 I_2} \cos \left( \frac{2\pi}{\lambda} \left( 2\Delta x \cos \left( \frac{\sqrt{x^2 + y^2}}{f} \right) \right) + \pi \right) \]  \hspace{1cm} (2.10)

where \( I_1 \) and \( I_2 \) are the intensities of the two beams, \( \lambda \) is the wavelength, and \( \Delta x \) is the path length difference between the two interferometer arms. The \( x \) and \( y \) are the coordinates in the focal plane of a lens of focal length \( f \).

If the light beam is of a single wavelength, fringes will be formed oriented perpendicular to the optical axis of the combined sub-beams. Fringes appear as alternating small rings of light and dark surrounding the light source. As the path difference increases, the fringes move outward and as the path difference decreases, the fringes move inward. Fig 2.7 shows an example of a fringe pattern that can be obtained with this kind of interferometer.

Figure 2.7: Example of a fringe pattern [12]
2.9.2 Mach-Zehnder Interferometry

A diagram of Mach-Zehnder interferometry is shown in Fig 2.8. A light beam is split into two sub-beams by a beam-splitter and then recombined by a second beam-splitter. Depending on the difference in the path lengths of the two sub-beams, constructive or destructive interference occurs. This interferometry is often used in quantum mechanics. If a beam traverses a path of length \( x \), then the phase is simply \( 2\pi \frac{x}{\lambda} \), where \( \lambda \) is the wavelength of the beam. If the two sub-beam path lengths are equal, then the phases are equal and constructive interference takes place \[13\].

Figure 2.8: Mach-Zehnder Interferometer.
According to physics of optics, on transmission, a wave does not make any phase shift. But on reflection it has a phase shift of $\pi$. The beam in the lower path in the interferometer undergoes one transmission and one reflection on its way from the light source to the second beam-splitter. The beam in the upper path goes through two reflections on its path from the light source to the second beam-splitter. So the lower path has a phase shift of $\pi$ but the upper path makes a phase shift of $2\pi$. Now if they continue on to the detector A, the lower path makes one more reflection and hence a total phase shift of $2\pi$. The upper path makes a transmission and, hence, the total phase shift remain at $2\pi$. So the two sub-beams interfere constructively. If the two sub-beams continue to the detector B, the lower path makes a phase shift of $\pi$ but the upper path makes a phase shift of $3\pi$. The phase difference is $2\pi$ and again they interfere constructively.

Let $l_1$ and $l_2$ be the total path lengths for the light traveling from the source to the detector for the upper and lower paths, respectively. The phase difference between the two paths on their way to detector A is

$$\delta = 2\pi \left( \frac{l_1 - l_2}{\lambda} \right) \quad \text{(2.11)}$$

Similarly the phase difference between the two paths on their way to the detector B is

$$2\pi + 2\pi \left( \frac{l_1 - l_2}{\lambda} \right) = 2\pi + \delta \quad \text{(2.12)}$$

If $\delta = 0$, there is constructive interference on both detectors A and B. By varying $\delta$, this condition can be changed and the probability of arrival at either detector is varied from 0 to 1. By having a phase detector, we can measure
the phase properties of the incoming wavefront by applying appropriate spatial filtering in one of the interferometer arms.

2.10 Phase Measurement Techniques

Instantaneous phase defines the current position of a periodical wave. When two signal are considered, the phase shift is defined as the constant difference between the two instantaneous phases, with one signal as a reference signal. The general expression for a wave is \( A \sin(2\pi ft + \phi) \) where \( A \) is the amplitude, \( f \) is the frequency and \( \phi \) is the phase of the wave. Frequency is defined as the rate at which the instantaneous phase changes.

By superimposing two waves, the waves can add to (in phase) or cancel out each other (out of phase). When the two waves have the same frequency and a different instantaneous phase, then they are considered to have a phase difference. If the phase difference is zero, the waves are said to be “in phase” with each other. But if the phase difference is 180 degrees, then the waves are said to be in “antiphase”. If the peak amplitudes of the two waves are equal and are in “antiphase”, then the superimposition of these two waves yields zero at all times. Phase difference ranges from 0 to 360 degrees. In-phase and anti-phase waves are shown in Fig 2.9. If a sinusoidal wave occurs ahead of the reference wave, then it is said to be leading in phase and if it occurs after the reference wave, then it is said to be lagging in phase with respect to the reference wave.

Phase is of high importance in communications and is used in schemes like phase-shift keying, where the phase of a reference signal is modulated in accordance with the data input. There are many techniques for phase estimation and a few of them are discussed in this section.
2.10.1 Zero Crossing Technique

The zero crossing technique is the most common method for measuring the frequency and phase of a periodic signal. Zero crossing is the instantaneous point at which the signal is zero and, for a sinusoidal signal, there will be two zero crossings per cycle. One occurs while going from positive to negative values and the other occurs while going from negative to positive values.

In the zero-crossing technique, a clock starts ticking when the reference signal passes through zero while going from positive to negative values and stops when the test signal passes through zero while going from positive to negative values. The time for which the clock runs gives the phase shift in time. The ratio of the time the clock runs to the period of the signal gives the phase shift of the
test signal in degrees ($\Delta \phi = \frac{\Delta t}{T} 2\pi$). The phase measurement is performed modulo $2\pi$. Phase measurement using zero crossings is illustrated in Fig. 2.10.

![Reference Signal](image)

Figure 2.10: Measurement of phase using zero-crossing technique.

In practice, the phase is measured over one or more time periods of the signal and then averaged. Measuring the phase over multiple periods helps to reduce errors caused by the phase noise as the perturbations at zero crossing will be small when compared to the total time of measurement [14]. This results in an accurate measurement but at the expense of slower measurement rate.

Usually the sinusoidal signals are greatly amplified to yield a square wave to improve the zero-crossing detection. Comparators are used to convert sinusoidal
signals into square signals. A dynamic hysteresis circuit can be added to these
comparators to reduce the probability of multiple zero-crossings and, hence, phase
errors.

2.10.2 Correlation Technique

The correlation technique is used to measure the degree to which two sig-
nals are related. A large positive or negative correlation value between two signals
represents a strong similarity between them. A zero correlation value between two
signals represents a small similarity between them. Cross correlation between two
signals \(x(t)\) and \(y(t)\) is given as

\[
R_{yx}(\theta) = \int_{-\infty}^{\infty} y(t)x(t + \theta)dt
\]

where \(\theta\) is the delay added to the signal \(x(t)\) when the comparison is made. If \(\theta\)
is zero, the correlation between the two signals is given by

\[
R_{yx} = \int_{-\infty}^{\infty} y(t)x(t)dt \quad (2.13)
\]

Let \(x(t)\) and \(y(t)\) be two sinusoidal signals of the same frequency \(f\) but
with different amplitudes \(A_1\) and \(A_2\), respectively. Then the two signals can be
written as

\[
x(t) = A_1 \cos(2\pi ft + \phi_1)
\]

\[
y(t) = A_2 \cos(2\pi ft + \phi_2)
\]

where \(\phi_1\) and \(\phi_2\) are phase shifts of signals \(x(t)\) and \(y(t)\) respectively. Multiplica-
tion of the two signals \(x(t)\) and \(y(t)\) yields
\[ x(t)y(t) = A_1 A_2 \cos(2\pi ft + \phi_1) \cos(2\pi ft + \phi_2) \]
\[ = \frac{A_1 A_2}{2} \cos(4\pi ft + \phi_1 + \phi_2) + \frac{A_1 A_2}{2} \cos(\phi_1 - \phi_2) \quad (2.14) \]

An integrator behaves as a low pass filter. The correlation can be implemented as shown in Fig 2.11. The signals \( x(t) \) and \( y(t) \) are multiplied by a multiplier and the resultant signal is passed through a low pass filter. Then the first term in (2.14) gets attenuated and only the second term which has a DC value gets through it. The resultant value is a cosine function of the phase difference between the two signals. The inverse cosine of the result gives the actual phase difference between the signals.

If the phase difference is zero, the correlation result will be maximum as \( \cos(0)=1 \). Thus if two signals have a phase difference of zero, the correlation value is maximum i.e., the two signals are very similar. If the phase difference is 90 degrees, the result of correlation is zero since \( \cos(90)=0 \). Thus the two signals do not have any similarity between them if the phase difference between them is
90 degrees. If the phase difference is 180 degrees, the correlation value is negative but very high. So, if two signals are in anti-phase, the similarity between them is high except that they have different polarities.

2.11 First Generation Integrated CMOS Optical Phase Sensor

Though integrated CMOS optical phase sensor was designed previously, there were some functional problems involved with that sensor. This sensor consists of an 8x8 array of pixels. Each pixel consists of a photodetector, a low pass filter and some other circuitry for processing the signals. The sensor also consists of two decoders and an 8-bit binary counter [15].

The low pass filter in each pixel of the previous generation phase sensor is built using an adaptive element. In the simulations of this sensor, the low pass filter performed well. In the layout of the low pass filter, there was a small hole left in the metal covering over the adaptive element. During the testing of the sensor, when it is exposed to light, the hole over the adaptive element allowed light to get through. This light was responsible for creating charges at the output node of the low pass filter. This caused the output voltage of the low pass filter to move. Thus, the hole in the metal covering over the adaptive element was responsible for the failure of the sensor.

In the previous generation sensor, the 8-bit binary counter was used as the reference clock. The pixels in the sensor sample the binary counter value. In the binary code counter, during the transition from one value to the next value, one or more output bits may change. If more than one output bit changes, it is unlikely that these bits switch states exactly at the same time. If the pixels sample during the transition from one state to another state, it may result in sampling of wrong value. One more disadvantage of this binary counter is that they consume lot of power.
Chapter 3

OPTICAL PHASE DETECTOR: ARCHITECTURE, DESIGN AND SIMULATIONS

3.1 Introduction

Measurement of phase of an optical wavefront is critical in many imaging applications. This kind of phase detector has many imaging applications, such as optical surface profiling, non-destructive testing and adaptive optical correction. For example when a uniform optical wavefront is reflected by an optical surface or medium, there will be deviations in phase of the wavefront due to variations of the surface. This is called optical surface profiling. Accurate measurement of the phase distribution across this wavefront gives an idea of the optical surface. As the optical signals are of very high optical frequency, accurate measurement of phase becomes very difficult in real time.

There are many techniques of measuring the phase. One measurement technique consists of two subsystems. The first subsystem introduces some temporal phase variation between two interfering beams. One is a reference beam which undergoes no phase deviations, and the second beam is the one that gets reflected. Here, the variation is obtained using an interferometric approach where the phase measurement accuracy is independent of the intensity variations across the wavefront. The second subsystem consists of an optical phase sensor to measure the phase of the time-varying interference pattern across an array of detection elements. An optical phase sensor is designed in this thesis and the design of this
sensor is discussed in this chapter. The integrated heterodyne optical sensor designed has phase calculation circuitry within the sensor and thus the phase can be calculated in real time easily. This on-chip measurement reduces the time for read-out and any additional components required for computation.

### 3.2 Architecture of Optical Phase Detector

The optical sensor developed here for the phase measurement application is an 8x8 array of pixels. The sensor also consists of a row decoder, a column decoder, a row driver, a column selector, a gray code counter and a gray-to-binary converter. The basic architecture of the optical phase sensor is shown in Fig 3.1.

The row decoder has 3 input lines and 8 output lines. Depending on the 3-bit row address at the input, one of the output select lines goes high, while the others remain low. The row driver block consists of some high strength buffers to drive all the row select transistors in a row. A 3-to-8 column decoder decodes the 3-bit column address to 8 output column select lines.

The gray code counter in the sensor is for generating a gray code sequence. The output of the 8-bit gray code counter is an 8-bit gray value corresponding to the count. This 8-bit gray value will be stored in pixels. The output of each pixel is 8-bit data. Outputs from all the pixels in a column are tied together, as only one row is selected at a time. So there will be 8 different outputs from 8 columns and the column selector selects one of the column outputs depending on which column select line is high. So, when row and column addresses are given, the output from the column selector is nothing but the output from the pixel at the intersection of the given row and column addresses. The output from the column selector will be an 8-bit gray value and a gray-to-binary converter converts this gray value to
its corresponding 8-bit binary value. This 8-bit binary value is buffered and sent off chip.

Each pixel consists of a photodiode with a load, a high pass filter, a comparator, edge-detection logic, 8 memory cells and 8 tristate inverters. A block diagram of each pixel is shown in Fig 3.2. When light is incident on a pixel,
the photodiode in that pixel converts the light into photocurrent. Photocurrent
developed by the photodiode is directly proportional to the intensity of the light
signal incident on that photodiode. The photodiode implemented here is formed
by \textit{n+}-diffusion in a \textit{p}-substrate. A load is connected in series with the photo-
diode to generate a voltage from the current. The load is two diode-connected
transistors that are operating in the subthreshold region of operation. For small
variations in current, the voltage will be proportional to the light signal on that
pixel. For large variations in current, the relationship between light and voltage is
non-linear. As the input light signal is a sinusoidal signal with frequency 10kHz,
the voltage developed will also be of the same frequency. This voltage has a DC
offset due to the threshold voltages of the load transistors and the average light
level. When the time-varying voltage is passed through a high pass filter, this off-
set is removed as the high pass filter blocks the DC component of the input signal.
Thus the output of the high pass filter is independent of the average illumination
level.

The output at the high pass filter is an analog signal with zero offset. When
this signal is compared to zero using a comparator, the output will be a square
wave with frequency 10kHz. Negative edges of this square wave are detected using
edge detection logic. At every negative edge, the gray code output from the gray
counter is stored in 8 SRAM cells. This stored value is read out through tristate
inverters whenever that particular row is selected.

An 8-bit resolution gray counter is designed to count from 0 to 255. Neg-
ative edges in the square wave output of the comparator appear at a frequency
of 10kHz. So, in one clock cycle of the square wave, the counter has to count
256 different values. Thus, the gray counter has to operate at a frequency that is
256 times the input light signal frequency. The clock frequency of the Gray code counter is therefore 2.56MHz for an input light signal at 10kHz frequency.

### 3.3 Photodiode with Load

If light of sufficient energy is incident on a reverse biased $p-n$ junction, the photocurrent varies almost linearly with the light flux \([16]\). In reverse bias, diodes have a huge parallel resistance. This resistance becomes smaller as the intensity of light falling on it increases. Diodes in reverse bias are more sensitive to light and are used as light detectors. There will be some photocurrent flowing through the photodiode when light is illuminated and there will also be some capacitance associated with the photodiode. So a photo diode can be modeled by a current source with capacitance in parallel to it. When a sinusoidal light signal of 10kHz is incident on the pixel, the photocurrent developed by the photodiode will also be sinusoidal of the same 10kHz frequency as photocurrent varies almost linearly with the light flux. This photocurrent is then converted into a voltage for
further processing. Consequently, a load has to be connected to the photodiode to generate a voltage which is related to the light flux.

![Photodiode with load](image)

**Figure 3.3: Photodiode with load.**

One way of conversion is by having a resistive load connected to the photodiode as shown in Fig 3.4. If the resistor used as the load is large, then the gain can be fairly large, but the response will be slow as the time constant given by \( \tau = RC \) is large. If a small \( R \) is chosen to reduce the time constant, the gain will also be reduced. Signal to noise ratio with this kind of load may also be unacceptable. For high \( R \), the layout area will also be high. The choice of \( R \) is very difficult, since photocurrents may vary from 100pA to 100nA and \( R = 10M\Omega \) for 1V drop.

One other way of converting the photocurrent into voltage is by connecting the photocurrent output to a transimpedence amplifier input. The photo current in a reverse-biased diode flows from \( V_{dd} \) towards \( V_{ss} \). Fig 3.5 shows the circuit connection for a transimpedance amplifier. A feedback resistor \( R_f \) is connected across the amplifier from the negative input to the output. One end of photodiode is connected to the negative input while the positive input is connected to ground.
As the gain of an amplifier is very high, no current flows into or away from the amplifier and the only path for current to flow is through the feedback resistor. The output of the transimpedance amplifier is given as $V_{out} = I_{ph}R_f$. By this method the voltage can be generated but the resistor, capacitor and the amplifier typically require a large layout area.

In a transimpedance amplifier, the response time is not $R_fX_C$, but considerably faster. The gain can also be large as large $R_f$ is used. The stability can be improved by having a large compensation capacitor in parallel to the resistor $R_f$. Thus transimpedance amplifiers have better SNR and better stability. But the disadvantage with this is that it occupies a lot of area considering the fact that there are total of 64 pixels and each would require one transimpedance amplifier. Thus, they are not used in this sensor.

One other good method of conversion is by having two diode-connected PMOS transistors as load as shown in Fig 3.6. A MOSFET operates as a small-signal resistor if its gate and drain are shorted. The transistor is always in saturation as both drain and gate are at the same potential ($V_{ds} = V_{gs}$). The drop
across each PMOS transistor is $V_{gs}(< V_{th})$. Consequently, the PMOS transistors are always in “saturated subthreshold” region, since both saturation condition $V_{ds} \geq V_{gs} - V_{th}$, and subthreshold condition $V_{gs} < V_{th}$ are satisfied \[5\]. The layout area for these diode-connected transistors is less than the area required for other methods and they can offer very high resistance. But these diode-connected PMOS transistors have non-linear resistance which depends on the photocurrent flowing through them \[7\]. The resistance of these transistors is given as

$$ R = \frac{1}{g_m} || r_0 \approx \frac{1}{g_m} $$  \hspace{1cm} (3.1)

where $g_m$, transconductance of the diode is given by

$$ g_m = \frac{\kappa I_d}{U_t} $$  \hspace{1cm} (3.2)
$I_d$ is the drain current of the transistor, $\kappa (=0.7)$ is the electrostatic coupling coefficient between the gate and channel and $U_t$ is the thermal voltage which is approximately $26mV$ at room temperature. For an average (DC) drain current of $10nA$, this resistance is calculated as $3.71M\Omega$. For average drains currents of $100nA$ and $100pA$, this resistance is $371k\Omega$ and $371M\Omega$ respectively.

![Photodiode schematic](image)

**Figure 3.6: Photodiode with diode-connected PMOS transistors as load**

From the above equations, the resistance is inversely proportional to the current flowing through the photodiode. Resistance offered by these transistors is pretty large and non-linear. So when the input light signal is sinusoidal, the output voltage will be a distorted sinusoid.

### 3.3.1 Transient Analysis

Fig 3.6 was simulated using a sinusoidal current source of frequency 10kHz. The transient analysis simulation result of this schematic is shown in Fig 3.7. The
signals are inverted from each other. In addition some delay can be seen between the input current and the output voltage. In transient analysis the current offset used is 10nA and the peak-to-peak current used is 10nA. The output voltage is not a perfect sinusoidal voltage but is inverted and slightly distorted. The output offset voltage was found to be $-542mV$ which is below two threshold voltage drops from $V_{dd}(=1.25V)$ considering the body effect for the lower diode-connected transistor. Output voltage swing was observed as $68mV$.

![Transient Response](image)

Figure 3.7: Transient analysis of photodiode with two diode-connected PMOS transistors as load, $V_{ss}=-1.25V$, $V_{dd}=1.25V$ and with a current source of frequency $10k$Hz as input.
3.3.2 AC Analysis

The size of the photodiode in the pixel is approximately 60$\mu$m by 60$\mu$m. The capacitance of each photo diode is calculated as

$$C_{ph} = C_J A + C_{JSW} P$$  \hspace{1cm} (3.3)

where $C_J = 0.426 fF/\mu m^2$ is the junction capacitance between the $n+$ and $p$-layers of the photodiode and $C_{JSW} = 0.301 fF/\mu m^2$ is the sidewall capacitance between the $n+$ and $p$- layers of the photodiode. $A$ and $P$ are area and perimeter of the $n+/p-$ photodiode respectively. Using (3.3) capacitance of the photodiode is calculated as 1.6pF.

As calculated previously, the resistance of the diode-connected transistors is 3.71M$\Omega$ for an average drain current of 10nA. The resistance of the two diode-connected transistors and the capacitance of the photodiode forms a low pass filter with a cutoff frequency given by

$$f_{c,ph} = \frac{1}{2\pi(2RC_{ph})}$$  \hspace{1cm} (3.4)

For the above values of R and $C_{ph}$, the bandwidth of the photodiode with load is evaluated as 13.4kHz. From simulations, the bandwidth is estimated as 19.4kHz. For smaller currents, the resistance increases and the the bandwidth decreases. Hence a photodiode current of at least 10nA is required in order to pass a 10kHz signal.

AC analysis simulation results of a photodiode with transistor load is shown in Fig[3.8]. From the AC analysis, the bandwidth was evaluated as 19.4kHz. The maximum voltage is around -26dB which is equivalent to $10^{-26/20} = 50mV$. In transient simulation, the output voltage swing was observed as 68mV for a DC
offset current of 10nA. Both simulation and calculated results are approximately equal. By increasing the intensity of the light signal, the drain current through the diode-connected loads also increases and the resistance of the load decreases since the load resistance is inversely proportional to the average drain current. As the bandwidth is inversely proportional to the resistance of the load, the bandwidth increases with increasing light intensity.

Figure 3.8: AC analysis of photodiode with diode-connected PMOS transistors as load, $V_{ss}=-1.25V$, $V_{dd}=1.25V$, $BW=19.4$kHz.

3.4 High Pass Filter

The cut-off frequency is defined as the frequency where the output power of the circuit is half of the maximum output power in the pass band or the frequency
where the gain of the circuit is 3dB less than the maximum gain of the circuit. A high pass filter is an electronic device or circuit that passes high frequency signals well, but attenuates frequencies lower than its cut-off frequency. High pass filters are very useful in circuits where the low frequency components are of no interest. A high pass filter blocks the DC component of the input signal.

### 3.4.1 Simple RC High Pass Filter

A simple RC high pass filter consists of a capacitor in series with the input signal and a resistor across the output as shown in Figure 3.9. At high frequencies, the capacitor has very low impedance and most of the input signal passes to the output. At low frequencies, the impedance of the capacitor increases and only a little of the input signal gets through the filter.

![Simple RC High Pass Filter](image)

\[
V_{\text{out}} = R \frac{R}{R + 1/j\omega C} V_{\text{in}}
\]

\[
H(j\omega) = \frac{V_{\text{out}}}{V_{\text{in}}} = \frac{j\omega RC}{1 + j\omega RC} \tag{3.5}
\]

The magnitude of \(H(j\omega)\) is given by
\[ |H(j\omega)| = \frac{1}{\sqrt{1 + 1/(\omega^2 R^2 C^2)}} \]

and the phase angle of \(H(j\omega)\) is given by

\[ \theta = \tan^{-1}(1/\omega RC) \]

and the cutoff frequency of the high pass filter is given as

\[ f_{cutoff} = \frac{1}{2\pi(RC)} \] (3.6)

### 3.4.2 Implementation

The sinusoidal light signal on the photodiode is converted into a photocurrent and the load across the photodiode converts this photocurrent to a sinusoidal voltage. But this sinusoidal voltage has an unknown non-zero DC offset and a several tens of millivolts of voltage swing. When this sinusoidal voltage is passed through the high pass filter, the DC component is blocked and the resulting output will be a sinusoidal signal with zero DC offset. The gain of the high pass filter at that input frequency may be less than \(1V/V\) or 0 dB resulting in decreased peak-to-peak output voltage.

The capacitor in this sensor is implemented using poly and poly2 layers. A capacitor of 100fF is used in the high pass filter. The schematic of the high pass filter implemented in each pixel is shown in Fig 3.10. An NMOS transistor operating in the subthreshold region acts as a resistor in the high pass filter. The mirroring circuit shown in the schematic is global to all the pixels. Bias current used in the mirroring circuit is 10nA. The multiplicity\((m)\) of the transistors \(M_3\)
and \( M_2 \) are 100 and 1, respectively. So a current of \( \frac{10nA}{100} = 0.1nA \) flows through transistor \( M_2 \). Similarly, the multiplicity of transistors \( M_1 \) and \( M_{pixel} \) are 10 and 1, respectively. So, the current in the NMOS transistor(\( M_{pixel} \)) of the high pass filter is 10pA. At such low currents, the transistor operates in the subthreshold region. The bias voltage \( V_{bias} \) is given to all the pixels. From 3.1 and 3.2, the resistance of the transistor \( M_{pixel} \) for a drain current of 10pA is calculated as 3.71G\( \Omega \).

![High Pass Filter schematic](image)

Figure 3.10: High pass filter schematic.

The input to the high pass filter is a sinusoidal signal with peak-to-peak voltage of around 80mV. Hence the \( V_{DS} \) voltage of this NMOS transistor does not
exceed 80mV. For $V_{DS} < 4U_t \approx 100mV$, where $U_T$ is the thermal voltage, the
transistor operates in linear region and the output is proportional to the input of
the high pass filter. Fig 3.11 shows the transient analysis of the high pass filter.
Input to the high pass filter is a sinusoidal voltage signal of offset -550mV and
peak-to-peak amplitude 80mV. From the simulation results, the output of the high
pass filter is a sinusoidal voltage signal with offset $V_{ss}(-1.25V)$ and peak-to-peak
amplitude of 25mV.

Figure 3.11: Transient analysis of High Pass Filter with a 10kHz sinusoidal signal
as input, $V_{ss}=-1.25V$, $V_{dd}=1.25V$. 
3.4.3 AC Analysis

AC analysis of the high pass filter is shown in Fig 3.12. From the AC analysis, the lower cutoff frequency of the high pass filter is observed as 291Hz and the gain in the pass band is around -9.8dB or 0.32 V/V. The capacitance used in the high pass filter is 100fF. The resistance of the transistor in the high pass filter is calculated as \(3.71 \Omega\). From 3.6, the cutoff frequency of the high pass filter is calculated as 428.9Hz. As the gain in the pass band is 0.32 V/V, for input peak-to-peak amplitude of 80mV, the output peak-to-peak amplitude has to be 25.6mV. From transient analysis, the output peak-to-peak amplitude is observed as 25mV. Both simulation and calculated results are approximately equal. By decreasing the mirroring current into the transistor, the lower cutoff frequency of the high pass filter also decreases.

3.5 Comparator with Hysteresis

The comparator implemented in this pixel is a three-stage comparator with internal hysteresis. The schematic for this is shown in Fig 3.13 [17]. This comparator consists of three stages. The first stage is the differential amplifier stage in which the differential input voltage is converted into differential current. This differential current is converted into output voltage using a current mirror. Common source amplifier is the second stage where the output voltage of the first stage is converted to a current. A current sink load to the common-source amplifier converts this current back to a voltage. This voltage is further amplified by the third stage which is a CMOS inverter [9].

The output voltage from the high pass filter is a sinusoidal signal with DC offset of \(V_{ss}\) and a peak-to-peak voltage of several tens of millivolts. This signal is given to the non-inverting input of the comparator. The reference voltage of \(V_{ss}\) is given to the inverting input of the comparator. If the differential pair of
the comparator is implemented with NMOS transistors, voltages less than $V_{ss}$ cannot keep them in the saturation region and therefore the comparator will not work for input voltages near to $V_{ss}$. Hence the differential pair is implemented with PMOS transistors M1 and M2. Thus for input voltages around $V_{ss}$, the comparator will work. Devices M3 and M4 form the current mirror to convert the differential current from the differential pair M1 and M2 into a single-ended voltage. Transistors M10, M11, M12 and M13 are used to introduce a small amount of hysteresis to the comparator. The amount of hysteresis can be varied by changing the hysteresis current $I_{hyst}$. 

Figure 3.12: AC analysis of High Pass Filter, $V_{ss}$=-1.25V, $V_{dd}$=1.25V, BW=291Hz.
Figure 3.13: Comparator with Internal Hysteresis.

For good matching of transistors, the sizes of M1 and M2 differential pair transistors are chosen as $W = 5.4\mu m$ and $L = 1.2\mu m$ with multiplicity $m=4$. Transistors M4, M5, M6, M10 and M11 are chosen as $W = 5.4\mu m$ and $L = 1.2\mu m$ with multiplicity $m=2$. $L = 1.2\mu m$ is selected for most of the transistors to make the comparator fast. $L$ is chosen as $0.9\mu m$ and $W$ is chosen as $5.4\mu m$ for M7 transistor with multiplicity $M=4$ to reduce the delay between the differential pair input and the gate of transistor M7. For the differential pair M12 and M13 used for introducing hysteresis, $W = 3.6\mu m$, $L = 0.9\mu m$ and $m=2$ are chosen. Transistors M8 and M9 in the inverter stage do not need good matching. So the
sizes are chosen as $W = 5.4\mu m$, $L = 0.6\mu m$, $m=2$ and $W = 5.4\mu m$, $L = 0.6\mu m$, $m=1$ for M8 and M9 respectively. A bias current $I_{bias}$ of $1\mu A$, hysteresis current $I_{hyst}$ of $47nA$ and supply voltages of $\pm 1.25V$ are used for the simulation.

In DC analysis, the inverting terminal (V-) is set to voltage $V_{ss}$ and the non-inverting terminal (V+) is swept from $-20mV$ to $+20mV$ with an offset of $V_{ss}$. The positive going hysteresis is measured as 4.4mv. If the non-inverting terminal is swept from $+20mV$ to $-20mV$ with an offset of $V_{ss}$, the negative hysteresis is measured as $-4.4mV$. The difference between these hysteresis values is defined as amount of the hysteresis which is calculated as $8.8mV$. By increasing the hysteresis current $I_{hyst}$, the amount of hysteresis increases. The DC sweep responses of the comparator for measuring positive hysteresis and negative hysteresis are shown in Fig 3.14(a) and Fig 3.14(b), respectively.

When a photodiode with diode-connected PMOS loads, high pass filter and comparator are connected together, then the input capacitance of one stage and the output capacitance of the previous stage interact. So after combining these three stages together, the outputs of each stage are affected. Fig 3.15 shows the transient analysis with all three stages combined. The input current is a sinusoidal signal with an offset of $10nA$ and a peak-to-peak amplitude of $10nA$. The output from the first stage is a slightly distorted sinusoidal voltage signal with the same frequency as that of the input current and with an offset of $-540mV$. Its peak-to-peak amplitude is $80mV$.

The output from the high pass filter is also a slightly distorted sinusoid signal. It has an offset of $-1.243V$ which is nearly equal to $V_{ss}(−1.25V)$ and a peak-to-peak amplitude of $57mV$. The output from the comparator stage is a square signal with the same frequency as that of the input current signal frequency. Due to the non-linearities in the first two stages, the duty cycle of the square signal

50
Figure 3.14: DC sweep of comparator with V- input set to Vss. Vdd = 1.25V, Vss = -1.25V, I_{bias}=1 \mu A, I_{hyst}=47 nA

is not exactly 50%. With these three stages combined together, the input current signal is converted to voltage square signal of same frequency. Also an inherent delay is introduced by the load, the low pass filter and the comparator. So the edges of the square wave are not exactly at zero crossings of the input signal.
Figure 3.15: Transient analysis of photodiode with load, high pass filter and comparator combined with input current of offset 10nA and peak-peak amplitude of 10nA, \( V_{dd} = 1.25 \) V, \( V_{ss} = -1.25 \) V.

3.6 Negative Edge Detection Logic

The output of the comparator in a pixel is a square wave with the same frequency as of the input light signal at that pixel. The frequency of the light signal on all the pixels is same but there may be some phase shift depending on the phase of the incoming signal. So the phase of the square wave from the comparator of all the pixels also differs. Thus it is required to detect an edge of
the square wave to estimate the phase. An 8-bit resolution counter is designed on
the chip that counts values from 0 to 255. The frequency of this counter must be
256 times the frequency of input light signal so that in one clock cycle of the input
light signal it can count values from 0 to 255. At every edge of the square wave
from the comparator, the counter value is stored in 8 SRAM cells for reading out
at some other time. Thus the counter value stored in each pixel corresponds to
the relative phase of the input light signal on that pixel.

Negative edge detection logic has been designed to detect the negative-going edges of the square wave. The schematic for the negative edge detection
logic is shown in Fig 3.16. The square wave from the comparator is passed through
three inverters I1, I2 and I3 to invert the square wave and introduce some delay.
Transistors with high length have large resistance and capacitance and thus a very
high delay. Instead of using a large number of inverters to introduce a large delay,
three high L inverters are used. The two inputs to the OR gate are the input
square wave and inverted and delayed version of the input square wave. So the
output of the OR gate is a pulse signal going low at negative edges of the input
square wave for a short duration and high during the remaining period. This pulse
signal is inverted using an inverter of strength 2 to drive more transistors. The
signal that comes out of this inverter is the output of edge detection circuit, which
is a pulse signal going high for a short duration at negative edges of the input
square wave and low during the remaining period. This pulse signal will have
the same frequency as that of the input light signal on that pixel. The transient
simulation results for the negative edge detection circuit is shown in Fig 3.17. The
pulse width of the signal from the edge detection circuit is measured as 21.55ns
in the simulations.
Figure 3.16: Negative Edge Detection Logic.

Figure 3.17: Transient simulation of Negative Edge Detection circuit, $V_{dd} = 1.25 \, V, V_{ss} = -1.25 \, V$.

3.7 Static RAM

Random Access Memory allows for the efficient organization of data in which the information is stored and read out of any data storage location in a random fashion without searching through a large amount of irrelevant data. The
two basic types of RAM’s are Dynamic RAM (DRAM) and Static RAM (SRAM). In DRAM the circuit has to be refreshed periodically, typically one thousand times per second. But SRAM need not be refreshed periodically and the memory values are retained as long as power is applied to the circuit. In SRAM the number of transistors required to hold the data is greater than the number of transistors for DRAM and therefore it occupies larger space and is costlier than DRAM. During readout, the capacitors used to store the data in DRAM cannot drive the column line. But in SRAM, the inverters are connected in a cross-coupled fashion to hold data and these inverters can drive the column lines high and low depending on the data at that particular location. This driving power makes SRAM circuitry faster.

The 8-bit counter value tapped at the negative edge of the square wave output of the comparator is stored in 8 SRAM cells. So each pixel requires 8 SRAM cells for storing the relative phase of the light signal on that pixel. The schematic for the SRAM block that was implemented in each pixel is shown in Fig 3.18. The pulse signal from the edge detection circuit is high for a very short duration and during this time transistors M1 and M2 in the SRAM cell are ON. When M1 and M2 are ON, the value on the input $D$ is passed on to the node $Z$ which is the output of the SRAM cell and the value on the input $D_{bar}$ is passed on to the node $Z_{bar}$. As the input $D_{bar}$ is an inverted version of $D$, the data at $Z_{bar}$ will also be an inverted version of $Z$. Cross-coupled inverters hold the data at $Z$ and $Z_{bar}$ for any period of time. Thus, there is no need for any refreshing circuitry. The transient simulation results for the SRAM circuit is shown in Fig 3.19.
3.8 Tristate Inverter

A tristate inverter is an inverter with two more transistors controlled by an enable signal. The schematic of the tristate inverter is shown in Figure 3.20. It has two NMOS transistors (M1 and M2) and two PMOS transistors (M3 and M4), all connected in series as shown in the schematic. Without the transistors M2 and M3, it is nothing but a normal inverter. The gate input of M2 is the enable input and the gate input of M3 is the inverted enable signal. When the enable input is high, M2 and M3 turn ON and the tristate inverter acts as an inverter. When enable input is low, M2 and M3 turn OFF and the output remains at the same state. When M2 and M3 are turned OFF there will not be any direct path for the output to go high or to go low. Due to the capacitance at the output node the value at the output is held and does not change much. This state is called a high impedance state. Thus when the enable input is high, the output is an
Figure 3.19: Transient simulation of SRAM circuit, $V_{dd} = 1.25\, V, V_{ss} = -1.25\, V$.

An inverted version of the input and when the enable input is low, the output is at high impedance state.

When a pixel is selected, the 8 SRAM bit values stored in that pixel have to be read out. There will be 8 row output select lines from the 3-8 row decoder and each row select line goes to all the 8 pixels in that corresponding row. At a time only one select line will be high and only one row will be chosen. This row select line acts as an enable signal input for the tristate buffers in the corresponding row. To read out the 8 SRAM bit values from a pixel, 8 tristate buffers are required for each pixel. So when a row is selected, all the 8 pixels in that row read out 8 bit values stored in the SRAM corresponding to the phase of the light signal on that pixel.
There are 8 pixels in a column and only one pixel gets selected when one of the rows is selected. So the 8 bit output buses from all the 8 pixels in a column are tied together. Therefore from each column an 8-bit output bus is the output and this bus goes to the column selector in which only one column output is selected.

3.9 Column Selector

As it was discussed an 8-bit output bus is the output from each column and the column selector selects the appropriate column resulting in a single 8-bit output digital value. The column selector consists of 64 tristate inverters. All the 64 output column bit lines act as data inputs to 64 different tristate inverters with the corresponding column select line output as the enable signal. The column decoder makes only one output select line high and the remaining low. The 8 output lines of the column decoder act as the enable signal for the
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Table 3.1: Truth table of 3-to-8 line decoder

tristate inverters. As only one column output select line is high, 8 tristate inverters are enabled and the remaining 56 are disabled. Thus, the output of the column selector is an 8-bit output digital value. As a Gray code counter is used for generating a Gray code sequence, the output of each pixel is a Gray code value. When a row and a column are selected, the 8-bit Gray code value corresponding to the phase of the light signal on the pixel at the intersection of the selected row and column is the output of the column selector. Thus, there is need of a Gray to binary code conversion circuit to convert the Gray code output value from the column selector to the corresponding binary value.

### 3.10 3-to-8 Line Decoder

A decoder is a combinational circuit that converts an $n$-bit binary code from $n$ input lines to a maximum of $2^n$ unique output lines. To select one pixel out of 8 rows or columns, a 3-to-8 line decoder has to be used. This decoder decodes three inputs into eight outputs, each representing one of the minterms of the 3-input variables. The outputs are mutually exclusive, as only one output will be high at a time. The truth table of a 3-to-8 line decoder is given in table 3.1.

The schematic of the 3-to-8 line decoder is shown in Fig 3.21. It has three inverters to provide complement of the three inputs $A$, $B$ and $C$. The eight AND
Figure 3.21: 3 to 8 decoder schematic.
gates generates 8 unique outputs. Depending on the three bit input, one of the row or column line is selected. For example, if the input code is 001, the second row or column is selected. Similarly if the input code is 111, the eighth row or column is selected. The sensor has two 3-to-8 decoders, one for row selection and the other one for column selection. Fig 3.22 shows the transient simulation results of the 3-to-8 line decoder. In the transient analysis it can be seen that only one output is high at a time and no two different input code bits select the same output.

Figure 3.22: Transient simulation of 3 to 8 decoder, $V_{dd} = 1.25\,V, V_{ss} = -1.25\,V$. 
### 3.11 Gray Code Counter

A Gray code counter is a counter in which only one output bit changes at a time. As two successive counts differ in only one bit, these counters have less switching noise when compared to binary counters in which multiple bits switch simultaneously. If a binary counter is sampled near the clock edge, some of the counter flip-flops may transition before others and can cause errors in sampling. But in a Gray code counter, as only one output bit changes at a time, asynchronous sampling has a maximum error of one count. In a correctly designed gray code counter there are no intermediate states and thus it is a glitch-free counter. In addition, Gray code counters have less power consumption.

At every negative edge detected by the edge detection logic of each pixel, the counter value is sampled and is stored in the 8-bit SRAM. As this asynchronous sampling has minimum error in gray code counters, a global 8-bit gray code counter is implemented.

The schematic of an 8-bit gray code counter is shown in Fig [3.23](#). It has an 8-bit binary counter followed by binary to gray conversion logic. At every clock edge of the binary counter, multiple output bits change one after the other but not exactly at the same time as all the output bits have different propagation delays. So the output of this binary to gray conversion logic is a gray code but with glitches at every clock edge. So this 8-bit gray code is sampled after all the output bit transitions of the binary counter and binary to gray conversions are finished. The clock signal for the binary counter is delayed by the time required for all the output bits of the binary counter to transition plus time for the binary-to-gray conversions. This delayed clock is used to sample the 8-bit gray code with glitches that is the output of the binary-to-gray conversion logic to get an 8-bit gray code without glitches.
3.11.1 Binary Counter

A binary counter is a digital sequential circuit that goes through a binary code sequence at every input clock edge. Binary counters are generally used for counting the number of times that an event has occurred and are constructed using flip-flops. Synchronous counters and ripple counters are two basic types of binary counters.

In a synchronous binary counter, all the flip-flops are operated in unison by having a common clock signal, so that all the output bits change state at the same time. But in ripple counters, or asynchronous counters, the output of the first flip-flop acts as the clock input to the second flip-flop and the output of this flip-flop acts as the clock input to the next flip-flop and so on. So, in a ripple counter all the output bits do not change state at the same time. A synchronous binary counter is a better counter than a ripple counter as all flip-flops are clocked at the same time.
An 8-bit synchronous binary counter counts values from 0 to 255 and is designed using 8 D flip-flops. The schematic of an 8-bit synchronous binary counter that is implemented as a binary counter is shown in Fig [3.24]. A common clock signal is given to all 8 D flip-flops. The outputs of all 8 D flip-flops are the output bits of the 8-bit binary counter. The output of the D flip-flop of every stage goes to one of the inputs of a half adder of the same stage. The sum output of the half adder goes to the data input of the D flip-flop of the same stage. The second input of the half adder in the first stage is $V_{dd}$ but for the other stages it is the carry output of the half adder of the previous stage. Thus 1 is added to the present number at every positive clock edge to get the next number in the binary sequence. Transient simulation results of the 8-bit synchronous binary counter with input clock frequency 2.56MHz is shown in Fig [3.25].

**D Flip-flops**

A D flip-flop typically has one data (D) input, one clock input and an output (Q). A D flip-flop is a digital circuit that stores the D input whenever its clock input transitions from low to high or from high to low. In a positive edge triggered D flip-flop, the data input is stored at each low-to-high clock input transition. The output (Q) shows the currently stored data. So this D flip-flop can be thought of as a basic memory cell. Since the data is shown at the output after some delay it is called as Delay flip-flop.

The schematic of a master-slave positive-edge-triggered D flip-flop implemented in the binary counter is shown in Fig [3.26]. This D flip-flop has one data input $D$, one clock input $Clk$, one $clearb$ input and a $Q$ output. If $clearb$ is set to low, the value at node $A$ will be low and if $clearb$ is set to high, the value at node $A$ will be the same as input $D$. If the clock input is low, the transmission gates T1 and T4 will be ON, while the transmission gates T2 and T3 will be OFF. The
Figure 3.24: Schematic of an 8-bit synchronous binary counter.
logic value at the node $A$ is shown at the node $B$ and $\overline{A}$ at the node $C$. When the clock goes high, T1 and T4 turn OFF, while T2 and T3 turn ON. Therefore the value at the node $C$ is an inverted version of the value at the node $A$ before the clock input goes high and remains at that state. The value at the node $C$ is available at the node $E$ and $\overline{C}$ at the output. Thus if $clearb$ is set to low, the output goes to low at the positive edge of the clock input irrespective of the input $D$. But if $clearb$ is set to high, the output is set to the input at the positive edge of the clock input.

Figure 3.25: Transient simulation of 8-bit synchronous binary counter, $V_{dd} = 1.25 \, V, V_{ss} = -1.25 \, V$, $clkfreq = 2.56 \, MHz$. 
Figure 3.26: Schematic of master-slave positive edge triggered D flip-flop \[19\].

Transient simulation result for the D flip-flop is shown in Fig \[3.27\]. When the clearb input is low, the output is low and does not depend on the data input. When the clearb is high, the output shows the data input value at the positive clock edge.

**Half Adder**

A half adder circuit has two one bit inputs, one sum output and one carry output. The truth table of a half adder is given in table \[3.2\]. When both the inputs are same, the sum output is low and when both the inputs are different, the output is high. So the sum output is an exclusive-or function of the inputs $A$ and $B$. The carry input is high only when both the inputs are high. The carry output is given by the AND function of both the inputs.
Figure 3.27: Transient simulation of positive edge triggered D flip-flop, $V_{dd} = 1.25\, V$, $V_{ss} = -1.25\, V$.

<table>
<thead>
<tr>
<th>Input A</th>
<th>Input B</th>
<th>Sum</th>
<th>Carry</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
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<td>1</td>
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<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

Table 3.2: Truth table of Half adder circuit

The schematic for the half adder circuit is shown in Fig 3.28. The XOR function and AND function are implemented using transmission gates. Transient analysis simulation results are shown in Fig 3.29.

3.11.2 Binary to Gray Converter

To develop the gray code sequence from the binary code sequence, a binary to gray code converter is needed. The general expression for the $n^{th}$ bit of a gray code output in terms of the binary code is given as $g_n = B_n \oplus B_{n+1}$ except for the most significant bit which is given by $g_n = B_n$. Figure 3.30 shows the schematic of the 8-bit binary to gray code converter. The exclusive-or of zero with any bit
Figure 3.28: Half adder schematic.

Figure 3.29: Transient simulation of half adder, $V_{dd} = 1.25 \, V, V_{ss} = -1.25 \, V$. 
gives the same bit as output. So the most significant gray code output is produced by the exclusive-or of the MSB of the binary code with \( V_{ss} \).

![Schematic of 8-bit Binary to Gray converter.](image)

The transient simulation results of the 8-bit gray code counter is shown in Fig 3.31. The frequency of the input clock to the gray code counter is 2.56MHz for the simulation. The frequency of the least significant bit \( Q_0 \) is measured as 640kHz and the most significant bit \( Q_7 \) is measured as 10kHz. In the simulation, only one output bit changed at every clock edge.

### 3.12 Gray to Binary Converter

The output of the column selector is an 8-bit gray code value and thus a gray-to-binary converter is needed to get an 8-bit binary value. The expression for converting an \( m \)-bit gray value to \( m \)-bit binary value is
Figure 3.31: Transient simulation of 8-bit gray code counter, $V_{dd} = 1.25 \, V$, $V_{ss} = -1.25 \, V$, $clk\,freq = 2.56 \, MHz$.

$$b_n = g_n \oplus g_{n+1} \cdots \oplus g_m = g_n \oplus b_{n+1} \quad \text{For } n < m$$

$$b_m = g_m$$

So only after the next highest significant bit is calculated, a particular bit can be calculated. The most significant bit of a binary value is the same as the most significant bit of an input gray value. The schematic of conventional gray-to-
binary converter is shown in Fig 3.32. For calculating the least significant bit in an 8-bit conversion, all the 7 most significant output bits have to be calculated and thus it requires a minimum of 7 exclusive-or operations. Hence, it takes a longer time for calculating the least significant bit than for calculating the other bits. But for the schematic of high-speed converter shown in Fig 3.33, it requires three exclusive-or operations. Thus the time required for calculating any output binary value remains the same.

In this circuit, parallel conversion takes place instead of the serial conversion which is used in normal conversion logics. One advantage of this kind of circuitry is that all the output bits are obtained almost at the same time. One more advantage is that the maximum time required for conversion is reduced from 7 exclusive-or operations to just 3 exclusive-or operations. But one disadvantage of this conversion is that in an $m$-bit conversion it requires $3m$ XOR gates instead of just $(m-1)$ XOR gates required in basic conversion logic.

When the output of the gray code counter is given as input to the gray-to-binary converter, the result must be a binary code sequence. Fig 3.34 shows the transient analysis simulation result when the output of the gray code counter is given as input to the gray-to-binary converter. From the analysis it can be seen that the output code is nothing but a binary code sequence. The clock frequency of the gray code counter is 2.56MHz. Hence the conversion with this kind of parallel circuitry works even at 2.56MHz. Thus, this circuit can be used for conversion of the 8-bit gray code column selector output into corresponding 8-bit binary code. The 8-bit output of the gray-to-binary converter represents the phase of the input light signal on the pixel selected using the row and column decoders.
Figure 3.32: Schematic of conventional 8-bit Gray to Binary Converter.
Figure 3.33: Schematic of high speed 8-bit Gray to Binary Converter.

3.13 Clever XOR Gate

A clever XOR gate is used for the exclusive-or operation in the gray-to-binary converter. The schematic of a clever XOR gate is shown in Fig. 3.35. The inverter I1 is used for generating $A\bar{b}$ from the input $A$. The truth table of the
Figure 3.34: Transient simulation of 8-bit binary counter using 8-bit gray code counter and gray-binary converter, $V_{dd} = 1.25\, V$, $V_{ss} = -1.25\, V$.

XOR gate is given in table 3.3. When the input $A$ is high, the transmission gate T1 turns OFF and the transistors M1 and M2 form an inverter with the input as $B$. So the output $Z$ is an inverted version of the input $B$ when the input $A$ is high. But when the input $A$ is low, T1 turns ON and the output $Z$ just follows the input $B$. Thus the operation of the clever XOR gate follows the truth table.

Transient simulation of the clever XOR gate is shown in Fig. 3.36. If both the inputs are same, the output is low and otherwise, the output goes high. XOR gates are generally used in comparing two bits. This XOR gate’s propagation
Figure 3.35: Schematic of Clever XOR Gate [19].

<table>
<thead>
<tr>
<th>Input A</th>
<th>Input B</th>
<th>output Z</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
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<tr>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

Table 3.3: Truth table of XOR circuit

delay from the input $A$ to the output $Z$ is different from the propagation delay from the input $B$ to the output $Z$.

3.14 Simulations

Fig 3.37 shows the simulation result for a single pixel. Signals $out_0 - out_7$ represent 8 output bits of the pixel where $out_0$ is the least significant bit and $out_7$ is the most significant bit. The bottom four signals in the figure are the counter output bits ($bit_0, bit_5, bit_6, bit_7$). Whenever the edge is detected, the counter values are tapped, stored in the memory and are immediately shown as the output bits. From the figure it can be seen that when the pulse signal is high,
Figure 3.36: Transient simulation of Clever XOR Gate, $V_{dd} = 1.25 \, V, V_{ss} = -1.25 \, V$.

The output bits switch to the state of their corresponding counter output bits. The edge is observed at $13.2 \, \mu s$. Time period of $100 \, \mu s$ is equivalent to count of 256. So, the equivalent count of $13.2 \, \mu s$ is $\frac{13.2 \times 256}{100} = 33.8$. From the simulations, the output is observed as $00100001(33)$. The simulation and calculated outputs are approximately equal.

Fig 3.38 shows the simulation results for 8X8 pixels. In one clock cycle of the input light signal, the counter counts 256 values. For a 10kHz light signal, the period of the signal is $100 \, \mu s$. If the pulse at the output of the edge detection logic in a pixel occurs at time $T$, then the count value stored in memory of that pixel is given by

$$\text{count value} = \text{floor} \left( \frac{256 \times (T \, \text{mod} \, 100)}{100} \right)$$
Figure 3.37: Transient simulation for single pixel for 10kHz light signal, $V_{dd} = 1.25\, V$, $V_{ss} = -1.25\, V$. 

In the simulation result shown in Fig 3.38, the pulse in the first pixel (first row, first column) occurs at 8.3$\mu$s. From the equation for the count value, the value stored in memory of the first pixel must be $\text{floor}(21.25) = 21$. When $r0$ (row0 and column0) signal is high, the value shown by the bits $op0 - op7$ corresponds to the count value stored in the row0, column0 pixel. So when $r0$ is high, the output $op0 - op7$ is 00010101(=21). The phase shift between the input signals on the two pixels is set to 50$\mu$s. So the edge in the second pixel occurs at 58.3$\mu$s and the count corresponding to it is floor(149.2)=149=10010101.
Figure 3.38: Transient simulation for 8X8 pixels for 10kHz light signal and phase shift of 50µs between two pixels, $V_{dd} = 1.25 \, V, V_{ss} = -1.25 \, V$.

It can be seen from the figure that for 50µs delay which is half of the input signal period, only the most significant bit changes. The difference the between binary outputs of the two pixels is 149-21=128. If $A$ corresponds to the binary output from one pixel and if $B$ corresponds to the binary output from another pixel, the phase shift in time between the input signals on those pixels is given as

$$delay = \frac{(A - B) \times 100 \mu s}{256}$$
Fig 3.39 shows the simulation result for 8x8 pixels with light signals of phase difference 8µs. The output on the first pixel is 00010101 (=21) and the output on the second pixel is 00101001 (=41). The difference between outputs on the two pixels is 41-21=20. The delay between these pixels is calculated as 7.8125 µs. The resolution of the sensor is 1 bit which is equivalent to $\frac{1 \times 100 \mu s}{256} = 0.39 \mu s$. Thus the measured and calculated values are within the resolution of the counter.

Figure 3.39: Transient simulation for 8X8 pixels for 10kHz light signal and phase shift of 8µs between two pixels, $V_{dd} = 1.25 V, V_{ss} = -1.25 V$. 
Chapter 4

LAYOUTS, TEST SETUP AND MEASUREMENT RESULTS

The optical wavefront phase sensor is fabricated in a 0.5µm CMOS technology through MOSIS. This sensor is an 8X8 pixel array. Each pixel is of size 110µmX110µm with a 60µmX60µm photodiode. The fill factor is approximately 30%. The sensor also has a row decoder, a column decoder, a gray counter and a gray-to-binary converter. Along with the phase measurement circuitry, a test photodiode was also laid out on the chip. Some test signal pins are taken out to verify the operation of each block. The layout of the whole chip, including digital and analog buffers is shown in Fig 4.1.

Each pixel consists of a photodiode, a high pass filter, a comparator, eight static memory cells and eight tristate output buffers. The layout of each pixel is shown in Fig 4.2. Analog and digital circuitry in the pixel have separate $V_{dd}$ and $V_{ss}$ supply rails. Analog outputs are taken out of the chip through analog buffers and digital outputs are taken out through digital buffers. These buffers are designed to drive large off-chip capacitive loads.

4.1 Test Setup

The chip is placed in a test box to shield it from noise. Fig 4.3 shows the test box with a phase measurement chip, a Digital Phase-Locked Loop (DPLL), power regulator circuitry and a virtual ground generation circuit. The power supply specifications used for the testing are $V_{dd} = 1.25V, V_{ss} = -1.25V$ and
Figure 4.1: Layout of the chip with digital and analog buffers. Dimensions: 1498µm x 1498µm.
Figure 4.2: Layout of a single pixel. Dimensions:110.1\(\mu m\) x 110.1\(\mu m\)

\(GND = 0V\). All the testing is done in a dark room to avoid perturbations from other light sources, such as lighting, overhead monitors etc.

As the phase measurement chip, the DPLL, the power regulator circuitry, the virtual ground generation circuitry and a few other components have to be placed in a single test box, all the circuits and components must be placed closed to each other. The battery in the test box is placed in a corner such that it does not interfere with the circuit connections. In the test box, four switches are used.
One switch is used to control the power supply from the battery and the others can be used for different purposes.

Figure 4.3: Test box with phase measurement chip, DPLL and other circuitries.

4.1.1 Regulated Power Supply Circuit

Noise generated in one part of the circuit may get coupled to the power supply and in turn may enter into other parts. A regulated power supply circuit prevents this noise coupling. The circuit diagram for a regulated power supply circuit is shown in Fig 4.4. A battery with a nominal input voltage of +9V is used to generate $V_{dd}$ equal to 2.5V. An LM317 adjustable 3-terminal positive regulator is capable of supplying in excess of 1.5A for outputs ranging from 1.2V to 37V. It employs internal current limiting, thermal shut-down and safe area compensation.
The circuit requires capacitors at the input and output to block any AC signals and to improve stability. The purpose of capacitor C0 is mainly to provide improved output impedance and rejection of transients. Capacitor Cin is required if the LM317 regulator is located away from the power supply filter. But since the input signal is DC, a battery, no filter capacitor is required. A potentiometer of value 1kΩ is used at the V_{ADJ} terminal to control the output V_{out}. The LM317 provides an internal reference voltage of 1.25V between the output and the adjustment terminal. The output voltage is given by

\[ V_{out} = 1.25V \left(1 + \frac{R_2}{R_1}\right) + I_{ADJ}R_2 \]

By adjusting resistor R_1, the output voltage is programmable. By setting the resistance R_1 to the minimum value, the regulator LM317 may get burned. So
it has to be observed that $R_1$ is never at the minimum value. Diode D1 is used to prevent the capacitor C1 from discharging through the internal low current paths and damaging the regulator. 9V from the battery is given as the input to this regulator circuit. But over a long time, the battery may fall to as low as 5.5V. By adjusting $R_1$, the output voltage is set to 2.5V. The output voltage of the regulated power supply circuit is measured using a digital multi meter (DMM). It should be ensured that all the wiring is done correctly and there are no loose connections before testing the circuit.

4.1.2 Virtual Ground Generation Circuit

A common problem in analog circuits is a requirement for a dual-voltage supply but the battery that is generally used is a single voltage supply. There are many ways of splitting the single supply to a dual supply. One easy way is by a resistor divider circuit as shown in Fig 4.5. The two 4.7kΩ resistors connected in series create a virtual ground. The output of this circuit is a voltage half-way between the input voltage and 0V. So, if the input voltage of the circuit is 2.5V, then the output voltage is 1.25V. As such, the voltage between the negative side of the power supply and the output is -1.25V and the voltage between the positive side of the power supply and the output is 1.25V. But this kind of circuit is prone to imbalance whenever $V_{GND}$ sinks or sources any current.

An alternate method of virtual ground generation circuit is shown in Fig 4.6. The LMC6482 is a CMOS dual rail-to-rail input and output operational amplifier. It provides a common-mode range that extends to both supply rails. It has an excellent common-mode rejection ratio and power supply rejection ratio. This op-amp is operated in a voltage follower configuration. A resistor divider circuit is connected at the non-inverting input terminal of the op-amp. Two matched resistors of value 100kΩ are used for the resistor divider circuit. The inverting
terminal of the op-amp is connected to the output of the op-amp. 9V supply from the battery is used for $V_{dd}$ of the op-amp.

Capacitors C1 and C2 are used at the input and at the output of the op-amp to reduce noise and to provide stability. This circuit generates an output voltage of 1.25V, which acts as a virtual ground for the whole test setup.

4.2 Electrical Testing

4.2.1 Current from the Test Photodiode

Apart from the phase measurement circuitry, a test photodiode is included on the chip. This test photodiode is a replica of the photodiode in each pixel with the same size and same pattern of metal lines and contacts over it. The layout of the test photodiode is shown in Fig 4.7. When the light is incident on the whole chip, the current from the test photodiode is comparable to the current from the individual pixels. The photocurrent generated by the test photodiode
is in nanoampere range. This current cannot be measured directly by a digital multi-meter (DMM).

To measure low currents, the current has to be converted into voltage. This conversion is accomplished by the circuit shown in Fig 4.8, using a transimpedance amplifier. The inverting terminal of the op-amp is connected to the output using the resistance $R$. The value of resistance $R$ is chosen typically around $10M\Omega$. The inverting terminal is connected to pin 9 ($I_{\text{pixel}}$) of the chip which is the photocurrent output of the test photodiode. The non-inverting terminal is connected to the virtual ground. The output voltage is measured across $V_{\text{Out}}$ and the virtual ground using a DMM. The photocurrent of the photodiode is then calculated using the equation

$$I_{IN} = \frac{V_{\text{Out}}}{R}$$
Figure 4.7: Layout of the test photodiode. Dimensions: 65.1µmx74.1µm
Thus for a given resistance $R$ and measured $V_{\text{out}}$, photocurrent $I_{IN}$ is obtained using this transimpedance amplifier.

Figure 4.8: Circuit to measure the photocurrent using a transimpedance amplifier.

### 4.2.2 Test Pixel

Individual blocks in the pixel need to be tested in order to verify current operation. Though there was enough space in the chip to lay out individual blocks, there were not enough pins for inputs and outputs for all the blocks. So the pixel in the first row and eighth column is used as a test pixel. From this pixel, a few important test signals are tapped and sent off-chip through pad buffers. Signals after the photodiode, the high pass filter, the comparator and the edge detection logic are taken out of the chip as shown in Fig 4.9.
If a sinusoidal light signal is incident on the test pixel, the voltage after the photodiode ($V_1$) and the voltage after the high pass filter ($V_2$) should be distorted sine waves due to the non-linear load. These signals are taken out of the chip through analog buffers. If the analog buffer is directly connected to the output of the high pass filter, the input capacitance of the analog buffer will be added to the comparator input capacitance. The effect on the operation of the high pass filter could be deleterious and consequently the results of the next stages will also be effected. So an NMOS transistor which acts as switch is placed in between the analog buffer and the high pass filter stage. When the gate input to this NMOS switch is high, the switch will be ON and the output of the high pass filter is
passed out of the chip through the analog buffer. Whenever the whole chip is tested, this NMOS transistor has to be switched OFF to avoid the addition of the input capacitance.

The output of the high pass filter is a distorted sinusoidal voltage signal with an offset of -1.25V, but the analog buffer does not work with its inputs around the negative rail voltage. Hence, it cannot buffer the output of the high pass filter. Thus, the signal after the high pass filter could not be tested.

The outputs after the comparator and edge detection logic are digital and so they are taken off chip through digital output buffers.

4.2.3 Column Decoder Testing

There are two 3-to-8 decoders on the chip. One is for row address decoding and the other is for column address decoding. Each decoder has 3 address inputs and 8 output select lines. Only one of the 8 output select lines will be high at a time. The column decoder is selected for testing the decoder operation. The column decoder’s first output select line is tapped off chip using a digital buffer. This select line must go high only for a column address of 000 and must be low for all other column addresses.

The decoder is tested for all 8 different combinations of the column address. It is observed that the first output select line goes high only when all the address inputs are at logic low. As the test results are similar to the simulation results, it is assumed that both decoders are working properly.

4.2.4 Gray Code Counter Testing

There is an 8-bit Gray code counter on the chip which is used as a reference clock for the phase measurement. The inputs for this counter are clock (pin 20) and clear (pin 21). The clear input is an active-high input. So, when it is connected to $V_{dd}$, the counter will be in reset state and, when it is connected
to $V_{ss}$, the counter will be in the active state. The counter is tested with clock signal that is a 2.56MHz square wave from a function generator.

Though the counter has 8 output bits, only the least significant and the most significant output bits are taken out of the chip for testing. When the counter is operated at a clock frequency of 2.56kHz, the least significant output bit of the gray code counter is a square wave of frequency 640kHz and the most significant output bit is a square wave of frequency 10kHz. Simulation results, expected results and the test results are almost similar and it can be concluded that the Gray code counter is working.

4.2.5 DPLL Testing

The Digital Phase Locked Loop (DPLL) chip is also placed in the test box along with the phase measurement chip. Both chips have common power regulator and virtual ground generation circuits. The DPLL can be used for generating the clock input signal for the 8-bit gray counter. The DPLL multiplies the frequency of the incoming clock signal by 256. A square wave of frequency 10kHz and peak-peak amplitude of $\pm 1.25V$ is given as the clock input for the DPLL. The DPLL generates an output square wave of frequency 2.56MHz.

4.3 Optical Testing

4.3.1 Testing with One LED

A red LED is used as the source of light for testing. A sinusoidal voltage of frequency 10kHz is given as the input signal for the LED. The most significant output bit (MSB) of the counter is used as the triggering source for the input light signal. For an input clock frequency of 2.56MHz, the MSB output of the counter is a square wave of frequency 10kHz. At every positive edge of the MSB square output, a new cycle of the input sine voltage starts with an initial phase of 0 degrees. Thus the input light signal is synchronized with the MSB output.
of the counter. By changing the phase delay value of the function generator, a
known amount of phase can be introduced to the incoming light.

The peak-to-peak and offset voltages for the input signal of the LED have
to be adjusted, in such a way that the light of the LED looks very bright. The
LED has to be held very close to the sensor in order to trigger the comparator.
Peak-to-peak and offset voltages of the function generator should be around 4.5V
and 3.5V, respectively, and should be varied depending on the responsivity of the
LED. Special care has to taken so that the LED does not make in contact with
the chip and accidentally break bonding wires of the chip. If an LED does not
trigger the comparator, a brighter LED has to be used for testing. LED used for
testing is red diffused 0.197inch diameter LED, part No:210825cL.

**Light Signal of Phase Zero**

Fig 4.10 shows the input light signal, MSB output of the counter and the
comparator output of the test pixel. When the sinusoidal light signal is incident
on the whole chip, the output of the comparator in the test pixel will be a square
wave. From the waveforms, the delay from the input voltage signal going low to
the comparator output of the test pixel going low is measured as 73µs.

As the negative edge detector is used in each pixel, at every negative edge
of the comparator output, the counter output value will be stored in the pixels.
As only one LED is being used, the light signal on all the pixels will be almost
the same and an identical count value will be stored in all the pixels. The start of
the counter is determined by the negative edge of the MSB output of the counter.

If the phase delay between the input light signal and the MSB output of the
counter is zero and the delay between the input light signal and the comparator
output of the test pixel is 73µs, the value stored in each pixel should be a count
value equivalent to 73µs. The time period of the light signal is 100µs which is
Figure 4.10: Zero phase delay between the input light signal and the MSB output of the counter.

equivalent to a count of 256. So the equivalent count for 73µs is \(\text{floor}(0.73 \times 256) = 186\).

The pixel in the first row and first column is selected using the row and column address lines. The output of the selected pixel is 101110xx where x is used to represent a bit which changes frequently. The decimal equivalent of the binary values 10111000 and 10111011 are 184 and 187, respectively. So the range of the output of the selected pixel is 184-187, which is very close to the expected value 186. Though the sensor is designed for an output resolution of 8 bits, the effective
resolution we can might be about 6 bits, as the output may vary between 2 to 4 values. Thus, the last one or two output bits may not give reliable information.

By changing the row and column addresses, different pixels can be selected. Fig 4.11 shows the outputs of different pixels. For pixel(2,2) the output is 10110xxx where x is used to represent a bit that changes frequently. From the output of other pixels it can be deduced that the output is changing between 2 to 4 values. For the value 10110xxx it can be assumed that the output might be varying between 10110000(176) and 10110111(183). So the average value of this output range is around 180. Thus from the output of the pixels, the range is calculated for all the pixels. Though the same light is incident on all the pixels, due to the mismatch between those pixels, the output of the pixels varies.

**Light Signal of Non-zero Phase**

The sensor has to be tested for different phase values of the light signal. The phase of the light signal is adjusted in the function generator in such a way that the input light signal leads the MSB output of the counter by $19\mu s$. The waveforms showing the input light signal, MSB output of the counter and output of the test pixel comparator are shown in Fig 4.12.

As the delay from the input light signal to the comparator output of the test pixel is $73\mu s$, the negative edge of the test pixel comparator output has to occur at $(73\mu s - 19\mu s = 54\mu s)$ after the cycle of MSB output of the counter starts. Thus the value stored in each pixel has to around $floor(0.54 \times 256) = 138$. The pixel in the first row and the first column is selected and the output of the selected pixel is observed as 1000110x. The range of this output is 140-141 which is close to the expected value of 138.

The phase of the light signal is adjusted to make the input light signal lag behind the MSB output of the counter by $32\mu s$ and the waveforms are shown in
<table>
<thead>
<tr>
<th>COLUMN ADDRESS</th>
<th>ROW ADDRESS</th>
<th>OUTPUT</th>
<th>RANGE</th>
<th>AVERAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>000</td>
<td>101110xx</td>
<td>184-187</td>
<td>185.5</td>
</tr>
<tr>
<td>001</td>
<td>001</td>
<td>10110xxx</td>
<td>176-183</td>
<td>179.5</td>
</tr>
<tr>
<td>010</td>
<td>010</td>
<td>101111xx</td>
<td>188-191</td>
<td>189.5</td>
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<td>011</td>
<td>011</td>
<td>101110xx</td>
<td>184-187</td>
<td>185.5</td>
</tr>
<tr>
<td>100</td>
<td>100</td>
<td>101100xx</td>
<td>176-179</td>
<td>177.5</td>
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<td>101</td>
<td>101</td>
<td>101101xx</td>
<td>180-183</td>
<td>181.5</td>
</tr>
<tr>
<td>110</td>
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<td>177.5</td>
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<td>111</td>
<td>111</td>
<td>101101xx</td>
<td>180-183</td>
<td>181.5</td>
</tr>
<tr>
<td>011</td>
<td>000</td>
<td>10111xxx</td>
<td>184-191</td>
<td>187.5</td>
</tr>
<tr>
<td>011</td>
<td>001</td>
<td>101101xx</td>
<td>180-183</td>
<td>181.5</td>
</tr>
<tr>
<td>011</td>
<td>010</td>
<td>1011100x</td>
<td>184-185</td>
<td>184.5</td>
</tr>
<tr>
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<td>011</td>
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<td>184-187</td>
<td>185.5</td>
</tr>
<tr>
<td>011</td>
<td>100</td>
<td>1011101x</td>
<td>186-187</td>
<td>186.5</td>
</tr>
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<td>101</td>
<td>1011100x</td>
<td>184-185</td>
<td>184.5</td>
</tr>
<tr>
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<td>110</td>
<td>101101xx</td>
<td>180-183</td>
<td>181.5</td>
</tr>
<tr>
<td>011</td>
<td>111</td>
<td>101110xx</td>
<td>184-187</td>
<td>185.5</td>
</tr>
</tbody>
</table>

Figure 4.11: Outputs of different pixels for a same light signal.
Figure 4.12: The input light signal leading the MSB output of the counter by 19µs.

Fig 4.13: As the light signal is of frequency 10kHz, the time period of the light signal is 100µs. The negative edge of the comparator output occurs $73\mu s + 32\mu s = 105\mu s \equiv 5\mu s$ after the cycle of the MSB output of the counter starts. The value that is expected to be stored in the pixels is $\text{floor}(0.05 * 256) = 12$. The output of the pixel in the first row and the first column is observed as 0001010x. The range
of this output is 20-21. In the similar way the outputs are observed for different phases of the input light signal.

Figure 4.13: The input light signal lagging behind the MSB output of the counter by 32µs.

Fig 4.14 shows the pixel output variation for different phases of an input light signal. The output of the pixel in the second row, second column and the output of the pixel in the fifth row, fifth column are observed for different values of the phase of the input light signal. The input light signal phase is varied in
steps of 15 degrees. A phase of 360 degrees is equivalent to $100\mu s$ in the time domain.

The graph for outputs at pixels (2,2) and (5,5) for different phase variations is shown in Fig 4.15. The solid line represents the expected output for different phase variations. From the graph, it can be concluded that the measured and the expected outputs are close.

4.3.2 Test Pixel

The output after the photodiode stage in the test pixel is a distorted sine wave for an input light source that is sinusoidal. Fig 4.16 shows the test results of the test pixel for sinusoidal input voltage of frequency 10kHz to the LED. The output is a distorted sine wave with some delay compared to the input. The offset of this output is -626mV which is nearly equal to $V_{DD}$ minus two threshold drops. The peak-to-peak amplitude of this output is 120mV.

The output after the high pass filter in the test pixel cannot be verified. It is a distorted sinusoidal signal with an offset of $V_{SS}$. The output of the comparator is a square wave and the test results shown in Fig 4.17 confirm this. The output square wave is of frequency 10kHz and 2.5V peak-to-peak amplitude, but it has delay of approximately $73\mu s$ from the input light signal.

The output of the edge detection block in the test pixel is a series of pulses of frequency 10kHz. At every negative edge of its input square wave, a short duration pulse is generated. The test results for the edge detection block are shown in Fig 4.18. The pulse duration is observed as 24ns.

4.3.3 Gray-to-Binary Converter

A Gray-to-Binary converter is used on the chip to convert the gray value that is stored in the pixels to their respective binary value. For testing, input bits 6 and 7 (LSB) of the Gray-to-binary converter are taken off chip. The output
<table>
<thead>
<tr>
<th>PHASE (DEGREES)</th>
<th>DELAY (µS)</th>
<th>OUTPUT AT PIXEL(2,2)</th>
<th>OUTPUT AT PIXEL (5,5)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>BINARY VALUE</td>
<td>RANGE</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>10110111</td>
<td>183</td>
</tr>
<tr>
<td>15</td>
<td>4.17</td>
<td>1100000x</td>
<td>192-193</td>
</tr>
<tr>
<td>30</td>
<td>8.33</td>
<td>1100111x</td>
<td>206-207</td>
</tr>
<tr>
<td>45</td>
<td>12.5</td>
<td>1101111x</td>
<td>222-223</td>
</tr>
<tr>
<td>60</td>
<td>16.66</td>
<td>111010xx</td>
<td>232-235</td>
</tr>
<tr>
<td>75</td>
<td>20.83</td>
<td>111101xx</td>
<td>244-247</td>
</tr>
<tr>
<td>90</td>
<td>25</td>
<td>00000010</td>
<td>2</td>
</tr>
<tr>
<td>105</td>
<td>29.17</td>
<td>0001000x</td>
<td>16-17</td>
</tr>
<tr>
<td>120</td>
<td>33.33</td>
<td>0001111x</td>
<td>30-31</td>
</tr>
<tr>
<td>135</td>
<td>37.5</td>
<td>001011xx</td>
<td>44-47</td>
</tr>
<tr>
<td>150</td>
<td>41.66</td>
<td>0011101x</td>
<td>58-59</td>
</tr>
<tr>
<td>165</td>
<td>45.83</td>
<td>010001xx</td>
<td>68-71</td>
</tr>
<tr>
<td>180</td>
<td>50</td>
<td>0100101x</td>
<td>74-75</td>
</tr>
<tr>
<td>195</td>
<td>54.17</td>
<td>010101xx</td>
<td>84-87</td>
</tr>
<tr>
<td>210</td>
<td>58.34</td>
<td>0101110x</td>
<td>92-93</td>
</tr>
<tr>
<td>225</td>
<td>62.5</td>
<td>0110010x</td>
<td>100-101</td>
</tr>
<tr>
<td>240</td>
<td>66.66</td>
<td>0110111x</td>
<td>110-111</td>
</tr>
<tr>
<td>255</td>
<td>70.83</td>
<td>01111xxx</td>
<td>120-127</td>
</tr>
<tr>
<td>270</td>
<td>75</td>
<td>10000xxx</td>
<td>128-135</td>
</tr>
<tr>
<td>285</td>
<td>79.16</td>
<td>1000100x</td>
<td>136-137</td>
</tr>
<tr>
<td>300</td>
<td>83.33</td>
<td>1001000x</td>
<td>144-145</td>
</tr>
<tr>
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<td>87.49</td>
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<td>330</td>
<td>91.66</td>
<td>1010011x</td>
<td>166-167</td>
</tr>
<tr>
<td>345</td>
<td>95.83</td>
<td>1010111x</td>
<td>174-175</td>
</tr>
</tbody>
</table>
Figure 4.15: Graph showing the measured and expected outputs for different phase variations.

bits of the Gray-to-binary converter are pins 37, 38, 39, 40, 1, 2, 3, 4. To test this converter, light is incident on the chip using an LED and after some time the LED is switched OFF. In this way, a constant value gets freezed in the RAM cells of the pixels and the converter can be tested by slowly observing the 2 inputs and the 8 output pins.

The output of the converter is observed as 11001110. The gray equivalent of this value is 10101001 which must be the input of the converter. The least significant input bit of the converter is pin 31 which is observed as 1. The next least significant bit of the converter is pin 30 which is observed as 0. These two
bits are same as the expected input bits. Thus, it can be concluded that the gray-to-binary converter is working.

4.4 Testing with a Light Signal of Frequency 10Hz

Testing is also done with a light signal of frequency 10Hz with a square wave voltage input. A square wave of frequency 10Hz and peak-to-peak amplitude 2.5V is given as the input to the LED. The frequency of the clock input for the counter should be 256 times the input light signal frequency. As the light signal is of frequency 10Hz, the clock frequency of the counter is given as 2.56kHz.

In a pixel, photodiode with the load acts as a low pass filter. As low pass filter passes low frequencies, for input light signal of frequency 10Hz, the output
Figure 4.17: Test results of the comparator in the test pixel for a sinusoidal light signal.

of the photodiode stage is a square wave of frequency of 10Hz but it is an inverted version of input signal. If the input to the high pass filter is a square wave of low frequency, the output of this filter is a series of spikes with the frequency same as that of input signal frequency. So the output of high pass filter stage is a series of spikes. Positive spikes at positive edges of the square wave and negative spikes at negative edges of the input square wave.

As the comparator in the pixel has hysteresis, the output of the comparator should be a square wave of frequency 10Hz. The output of edge detection stage in the pixel is a series of short duration pulses with frequency 10Hz. This pulses are
Figure 4.18: Output of the edge detection block in the test pixel for a sinusoidal light signal.

used to sample the 8-bit gray code counter output. Fig 4.19 shows the waveforms of input square wave, photodiode output, high pass filter output, comparator output and edge detection circuit output. These waveforms are drawn neglecting the delay of each block.

For phase delay of zero between input light signal and MSB output of the counter, outputs of comparator in the test pixel and MSB output of the counter are shown in Fig 4.19. The delay between negative edges of both outputs is 2.32ms. Time period of this light signal is 100ms which is equivalent to output of 256. The
delay of 2.32ms is equivalent to \(\text{floor}(0.0232 \times 256) = 5\). The measured output of the pixel(1,1) is 0000101(5) which is same as the expected output.
4.5 Testing with Two LED’s

While testing the chip with one LED, the same light signal is incident on all the pixels. So the output of all the pixels is almost the same for a fixed phase light signal. Two different light signals cannot be incident on two different pixels by directly placing the LEDs over the chip. Fig 4.20 shows the test setup for making two light signals from two LEDs be incident on two different pixels. Thus, after introducing a phase difference between the two light signals, two different outputs are produced. From the difference between these two outputs, the phase difference can be estimated.

The two LEDs in the test setup are soldered on a general purpose circuit board. The circuit board is cut in such a way that it fits in the cylindrical aluminium tube that is shown in Fig 4.21. The microscope seen in the test setup has two eyepieces. One of the eyepieces is replaced by the cylindrical tube and the light pattern from LEDs is observed from the other eyepiece. The LEDs and the tube are adjusted such a way that the LEDs are close to the lens of the microscope. The testbox is placed under the microscope and is adjusted so that the light from the microscope falls on the sensor. The light is made to be focused on the sensor by adjusting the height of the microscope.

The input clock signal for the gray code counter in the sensor is a square wave of frequency 2.56MHz. The MSB output of the counter is a square wave of frequency 10kHz. This signal is used to synchronize the 10kHz sine wave signals for the two LEDs. The setup for synchronizing the two LEDs with the input clock is shown in Fig. 4.22. The phase shift of either light signals can be varied and thus a phase difference can be induced between the two light signals.

If analog function generators are used for generating light, the 10kHz square wave from the counter can directly trigger these function generators. But the
phase of these analog function generators cannot be adjusted accurately. The main disadvantage of using two analog function generators is that the output resistance of the function generators may not be the same and thus we may not
generate two identical light signals. The analog function generator used in testing is wavetek, Model No:143.

With digital function generators (Agilent, Model No:33120A), the square wave from the MSB of the counter can not trigger them. Square waves of peak-to-peak amplitudes greater than 3V can only trigger these function generators. So a BJT inverter is used to generate the square wave output of peak-to-peak amplitude greater than 3V from the square wave of the counter.
Figure 4.22: Setup for synchronizing the two LEDs.

**BJT Inverter**

The circuit diagram for the BJT inverter is shown in Fig. 4.23. The input for this inverter is a square wave of frequency 10kHz and peak-to-peak amplitude of 2.5V. So the input for this circuit will be either high or low. When the input is low, the base-emitter junction is reverse-biased and current $I_B = 0$. Thus the transistor is in the cutoff region and $I_C = 0$. So the voltage drop across the resistor at collector is zero and thus $V_{out} = 7.75V$.

When the input is high, the base-emitter junction is forward biased and the transistor is driven into saturation region. The output is equal to $V_{CE(sat)}$ which is around 0.2V. The test results for this inverter are shown in Fig 4.24. The input square wave is of frequency 10kHz and 2.5V peak-to-peak amplitude. The
output is inverted version of the input but with a peak-to-peak amplitude of 6V. This output signal is used to trigger the two digital function generators.

By varying the phase on both the function generators, a phase difference can be induced between the two light signals. These non-identical light signals from the LEDs are incident on two different sections of the chip as shown in Fig 4.25. The outputs at both the sections are noted by changing the addresses of both row and column decoders appropriately.

One of the light signals is incident on a section of the chip with pixel (2,2) as the center and this light signal is kept at phase zero. The other light signal is incident on a section with pixel (7,7) in the center. The phase of this second signal is varied from zero to 345 degrees in steps of 15 degrees and the outputs from pixel (2,2) and pixel (7,7) are noted. Fig 4.26 shows the outputs for pixel (2,2) and pixel (7,7) for various phase difference values.
From the Average values at both pixels (2,2) and (7,7), output difference is calculated. The plot for both measured and expected output differences is shown in Fig 4.27. The solid line represents the expected output difference and the dots represent the measured output difference. The expected output difference and the measured output difference are close for all the phase variations.

4.6 Output Bit Resolution

From Fig 4.26, the output of the pixel(7,7) for phase variation of 135 degrees is 11xxxxxx. As the 6 least significant bits are varying, the output range is calculated as 192-255. Though only the last 1 or 2 bits varied for most of the phase values, we can not conclude that the output bit resolution is 6 bits. So testing is done to determine the output bit resolution.
In this testing, least significant bits 1 and 2 are observed on one oscilloscope and the next least significant bits 3 and 4 are observed on other oscilloscope. An external trigger is applied to these oscilloscopes such a way that the waveforms on these oscilloscopes gets freezed once every ten seconds. These freezed values are observed to determine the possible outputs of the pixel.
<table>
<thead>
<tr>
<th>BINARY VALUE</th>
<th>RANGE</th>
<th>AVERAGE</th>
<th>PHASE VARIATION OF LIGHT SIGNAL ON PIXEL(7,7) (in degrees)</th>
<th>BIN</th>
<th>RANGE</th>
<th>AVERAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>010011xx</td>
<td>76-79</td>
<td>77.5</td>
<td>0</td>
<td>0100111x</td>
<td>78-79</td>
<td>78.5</td>
</tr>
<tr>
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<td>76-79</td>
<td>77.5</td>
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<td>01000xxx</td>
<td>64-71</td>
<td>67.5</td>
</tr>
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<td>76-79</td>
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<td>001101xx</td>
<td>52-55</td>
<td>53.5</td>
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<td>00011xxx</td>
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<td>000000xx</td>
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<td>1.5</td>
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<td>77.5</td>
<td>105</td>
<td>1111xxxx</td>
<td>240-255</td>
<td>247.5</td>
</tr>
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<td>77.5</td>
<td>120</td>
<td>11101xxx</td>
<td>232-239</td>
<td>235.5</td>
</tr>
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<td>11xxxxxx</td>
<td>192-255</td>
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<td>1101010x</td>
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<td>77.5</td>
<td>285</td>
<td>1000001x</td>
<td>130-131</td>
<td>130.5</td>
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<td>77.5</td>
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<td>011110xx</td>
<td>120-123</td>
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<td>76-79</td>
<td>77.5</td>
<td>315</td>
<td>0110110x</td>
<td>108-109</td>
<td>108.5</td>
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<td>76-79</td>
<td>77.5</td>
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<td>011000xx</td>
<td>96-99</td>
<td>97.5</td>
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<td>77.5</td>
<td>345</td>
<td>0101100x</td>
<td>88-89</td>
<td>88.5</td>
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<td>010011xx</td>
<td>76-79</td>
<td>77.5</td>
<td>360 or 0</td>
<td>0100110x</td>
<td>76-77</td>
<td>76.5</td>
</tr>
</tbody>
</table>

Figure 4.26: Outputs of pixel(2,2) and pixel(7,7) for various phase difference values.

Phase variation is adjusted such a way that only last 4 bits are varying and the first 4 bits are fixed. As the last 4 bits vary, there are total of 16 possible outputs. These last 4 bits are observed on 2 different oscilloscopes. The values
on oscilloscopes gets freezed once every 10 seconds. From many observations, it is observed that the possible values on these last 4 bits are 0110, 0111, 1000. Thus, the output is changing just between 3 values.

Next, the phase is adjusted such a way that last 5 bits vary and the first 3 bits are fixed. The possible values observed on these last 5 bits were 10001, 10000, 01111, 01110. Values 10001 and 01110 are observed only once or twice in 50 observations. Similarly, the phase is adjusted to have only last 3 bits varying. The possible last 3 bits observed for this phase value are 010, 011, 100.
From this testing, it can be concluded that the output value for any phase value varies between 2-4 values. Thus, it can be concluded that the output bit resolution is 6-7 bits.
Chapter 5

CONCLUSIONS, APPLICATIONS AND RECOMMENDATIONS

5.1 Conclusions

The motivation of this thesis is to design a second generation optical phase sensor. This sensor is used to detect the phase across the incoming optical wavefront. Phase calculation circuitry is integrated within the sensor to measure the phase at real time without any additional hardware.

The drawbacks in the first generation sensor are discussed and the solutions for those drawbacks are provided. Even this second generation sensor consists of an 8x8 array of pixels. One of the improvements made to the sensor is that Gray-code counters are used instead of binary counters and a novel technique of converting an 8-bit Gray code to an 8-bit Binary code is implemented. The design and simulations results for the individual blocks and for the sensor are discussed. Layout of the analog blocks in each pixel is done using common-centroid technique to reduce mismatch and offset errors. This sensor was sent to MOSIS for fabrication in a 0.5µm CMOS technology.

A test setup is built using a microscope, an aluminium cylindrical tube and two LEDs. The phase detector chip is placed in a test box in order to shield it from external noise. Light signals from two LEDs are focused on the chip using a microscope. Each LED light spot is incident on a particular pixel such that it covers the whole pixel. Supply voltages of ±1.25V. are used for the test setup.
Static and dynamic testing is done on the sensor and the measurements are made. These measurement results are compared with simulation results and it was observed that these results are consistent. This confirms the correct operation of the sensor.

5.2 Applications

This sensor has many imaging applications where the phase of the optical signal is critical. Such applications include optical surface profiling, non-destructive testing and adaptive optical correction. When a uniform optical wavefront is reflected by an optical surface or medium, there will be deviations in the phase of the wavefront due to the variations of the surface. This is called optical surface profiling. Accurate measurement of the phase distribution across this wavefront gives an idea of the optical surface.

In areas such as construction, manufacturing and aviation, testing for defects in an object has to done without destroying the test object. This is called non-destructive testing. In this testing an optical wavefront is incident on the test object and the phase of the reflected optical wavefront is measured by this sensor. This helps in finding any defects such as cracks and corrosion.

5.3 Recommendations

The optical phase sensor is tested for different phase values but this testing is done only once. Repeatability of the testing has to be checked to see if the same range of outputs can be measured for the same phase of the input light signal.

The output of the high pass filter in the test pixel could not be measured as the output of analog buffer cannot be operated at around V_{ss}. So the operation of the high pass filter could not be tested. So a method has to be designed to fix this problem and observe the output of the high pass filter. Thus, operation of the high pass filter can be tested.
The testing is done with two LEDs by forming a simple time-varying pattern. By using interferometric techniques, a complex fringe pattern can be formed and the testing can be done with this light pattern. Data acquisition devices can also be used to acquire the outputs at real time. Even the selection of the pixels can be done using this devices. Using a computer, the outputs can be studied and the phase of optical wavefronts can be measured at real time. It can be implemented in adaptive optics system for correction of aberrations at 10kHz sampling rate.

High pass filter in a pixel attenuates some of the input signal and the voltage swing at the output of the high pass filter is low. It can redesigned such a way that larger output swings are obtained at input and output of the high pass filter. Thus the sensor can work even for low light levels. Array size of the sensor can also be increased to 64x64 pixels.
APPENDICES
Appendix A

LAYOUTS AND TEST SETUP

The layouts of all individual blocks and the whole chip are shown. A micrograph of the chip is also shown in Fig. A.8.

Figure A.1: Layout of the whole chip including buffers
Figure A.2: Layout of a Single Pixel
Figure A.3: Layout of 8-bit Gray Code Counter

Figure A.4: Layout of 3-to-8 decoder
Figure A.5: Layout of 8-bit Gray-Binary Converter

Figure A.6: Layout of Edge detection circuit
Figure A.7: Layout of test photodiode
Figure A.8: Micrograph of the Chip
Figure A.9: Shielded test box
Appendix B

PIN OUT AND TEST PROCEDURE FOR THE INTEGRATED CMOS OPTICAL PHASE SENSOR

B.1 PIN OUT

Pin out of the integrated CMOS optical phase sensor is

<table>
<thead>
<tr>
<th>Pin #</th>
<th>Pin Name</th>
<th>Description</th>
<th>Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>op3</td>
<td>Output bit 3</td>
<td>O - Digital buffer</td>
</tr>
<tr>
<td>2</td>
<td>op2</td>
<td>Output bit 2</td>
<td>O - Digital buffer</td>
</tr>
<tr>
<td>3</td>
<td>op1</td>
<td>Output bit 1</td>
<td>O - Digital buffer</td>
</tr>
<tr>
<td>4</td>
<td>op0</td>
<td>Output bit 0</td>
<td>O - Digital buffer</td>
</tr>
<tr>
<td>5</td>
<td>vdd(digital)</td>
<td>Vdd for digital blocks</td>
<td>I/O - Protected</td>
</tr>
<tr>
<td>6</td>
<td>vdd(Analog buffer)</td>
<td>Vdd for analog buffers</td>
<td>I/O - Vdd pad</td>
</tr>
<tr>
<td>7</td>
<td>Ibiasp</td>
<td>Bias current for PMOS to generate bias voltage for analog buffers</td>
<td>I - Ibiasp pad</td>
</tr>
<tr>
<td>8</td>
<td>Imirror</td>
<td>Mirroring current for all the High Pass filters in all the pixels</td>
<td>I - Bare pad</td>
</tr>
<tr>
<td>9</td>
<td>Ipixel</td>
<td>Output current of the test photodiode</td>
<td>O - Bare pad</td>
</tr>
<tr>
<td>10</td>
<td>Vhpf</td>
<td>Voltage at output of the High Pass filter in the test pixel</td>
<td>O - Analog Buffer</td>
</tr>
<tr>
<td>11</td>
<td>Vph</td>
<td>Voltage at input of the High pass filter in the test pixel</td>
<td>O - Analog Buffer</td>
</tr>
<tr>
<td>12</td>
<td>Ibias</td>
<td>Bias current to provide bias voltages for comparators in all the pixels</td>
<td>I - Bare pad</td>
</tr>
<tr>
<td>13</td>
<td>Ihyst</td>
<td>Hysteresis current for comparators in all the pixels</td>
<td>I - Bare pad</td>
</tr>
<tr>
<td>14</td>
<td>Ibiasn</td>
<td>Bias current for NMOS to generate bias voltage for analog buffers</td>
<td>I - Ibiasn pad</td>
</tr>
<tr>
<td></td>
<td>Vss (Analog buffer)</td>
<td>Vss for analog buffers</td>
<td>I/O - Vss pad</td>
</tr>
<tr>
<td>---</td>
<td>-------------------</td>
<td>------------------------</td>
<td>---------------</td>
</tr>
<tr>
<td>16</td>
<td>Vdd (Digital buffer)</td>
<td>Vdd for digital buffers</td>
<td>I/O - Vdd pad</td>
</tr>
<tr>
<td>17</td>
<td>row1</td>
<td>Input 1 for the row decoder</td>
<td>I - Protected</td>
</tr>
<tr>
<td>18</td>
<td>row2</td>
<td>Input 2 for the row decoder</td>
<td>I - Protected</td>
</tr>
<tr>
<td>19</td>
<td>row3</td>
<td>Input 3 for the row decoder</td>
<td>I - Protected</td>
</tr>
<tr>
<td>20</td>
<td>clk</td>
<td>Clock input for the counter</td>
<td>I - Protected</td>
</tr>
<tr>
<td>21</td>
<td>clear</td>
<td>Clear input for the counter</td>
<td>I - Protected</td>
</tr>
<tr>
<td>22</td>
<td>col3</td>
<td>Input 3 for the column decoder</td>
<td>I - Protected</td>
</tr>
<tr>
<td>23</td>
<td>col2</td>
<td>Input 2 for the column decoder</td>
<td>I - Protected</td>
</tr>
<tr>
<td>24</td>
<td>col1</td>
<td>Input 1 for the column decoder</td>
<td>I - Protected</td>
</tr>
<tr>
<td>25</td>
<td>Vss (Digital buffer)</td>
<td>Vss for digital buffers</td>
<td>I/O - Vss pad</td>
</tr>
<tr>
<td>26</td>
<td>Vswitch</td>
<td>Input for Nmos switch to select the output of High Pass filter of test pixel</td>
<td>I - Protected</td>
</tr>
<tr>
<td>27</td>
<td>count0</td>
<td>Counter output bit 0 (LSB)</td>
<td>O - Digital buffer</td>
</tr>
<tr>
<td>28</td>
<td>count7</td>
<td>Counter output bit 7 (MSB)</td>
<td>O - Digital buffer</td>
</tr>
<tr>
<td>29</td>
<td>dec0</td>
<td>Output bit 0 for the column decoder</td>
<td>O - Digital buffer</td>
</tr>
<tr>
<td>30</td>
<td>bin6</td>
<td>Input bit 6 for the Gray-Binary converter</td>
<td>O - Digital buffer</td>
</tr>
<tr>
<td>31</td>
<td>bin7</td>
<td>Input bit 7 for the Gray-Binary converter</td>
<td>O - Digital buffer</td>
</tr>
<tr>
<td>32</td>
<td>Vedge</td>
<td>Output after the edge detection circuit in the test pixel</td>
<td>O - Digital buffer</td>
</tr>
<tr>
<td>33</td>
<td>Vsquare</td>
<td>Output after the comparator in the test pixel</td>
<td>O - Digital buffer</td>
</tr>
<tr>
<td>34</td>
<td>Vdd (analog)</td>
<td>Vdd for analog blocks</td>
<td>I/O - Protected</td>
</tr>
<tr>
<td>35</td>
<td>Vss (analog)</td>
<td>Vss for analog blocks</td>
<td>I/O - Protected</td>
</tr>
<tr>
<td>36</td>
<td>Vss (digital)</td>
<td>Vss for digital blocks</td>
<td>I/O - Protected</td>
</tr>
<tr>
<td>37</td>
<td>op7</td>
<td>Output bit 7</td>
<td>O - Digital buffer</td>
</tr>
<tr>
<td>38</td>
<td>op6</td>
<td>Output bit 6</td>
<td>O - Digital buffer</td>
</tr>
<tr>
<td>39</td>
<td>op5</td>
<td>Output bit 5</td>
<td>O - Digital buffer</td>
</tr>
<tr>
<td>40</td>
<td>op4</td>
<td>Output bit 4</td>
<td>O - Digital buffer</td>
</tr>
</tbody>
</table>
B.2 Suggested Test Procedure

For split supplies: \( V_{dd} = +1.25V \) (logic 1), \( AG_{nd} = 0V \), \( V_{ss} = -1.25V \) (logic 0)

For single supply: \( V_{dd} = +2.5V \) (logic 1), \( AG_{nd} = 1.25V \), \( V_{ss} = 0V \) (logic 0)

Test Engineer:
Test Date:
Chip ID:

1. Connect \( V_{dd} \) to pin 5, pin 6, pin 16, pin 34.

2. Connect \( V_{ss} \) to pin15, pin 25, pin 35, pin 36.

3. Attach nominally 14kΩ resistor from \( V_{dd} \) to pin \( I_{biasn} \) (pin 14) to establish a 100 \( \mu A \) current source. The current is split two-ways (50 \( \mu A \) each) for each of the two analog output buffers.

4. Attach nominally 12kΩ resistor from \( V_{ss} \) to pin \( I_{biasp} \) (pin 7) to establish a 100 \( \mu A \) current source. The current is split two-ways (50 \( \mu A \) each) for each of the two analog output buffers.

5. Attach 15.6MΩ resistor from \( V_{ss} \) to pin \( I_{mirror} \) (pin 8) to establish 100nA current source. The current is used to bias all high pass filters.

6. Attach 23.4kΩ resistor from \( V_{ss} \) to pin \( I_{bias} \) (pin 12) to establish 64\( \mu A \) current source. The current is used to bias all comparators.

7. Attach nominally 187.5kΩ resistor from \( V_{ss} \) to pin \( I_{hyst} \) (pin 13) to establish 8\( \mu A \) current source. The current is used to program the hysteresis of the comparators.
8. Connect Vss to pins row1(pin17), row2(pin 18), row3(pin 19), col3(pin 22), col2(pin 23), col3(pin 24), clear(pin21).

9. Testing counter: Apply square wave of frequency 2.56MHz and amplitude \( \pm 1.25V \) at pin clk(pin 20) and observe outputs at pin count0(pin 27) and pin count7(pin 28).

10. Testing column decoder: output at pin dec0(pin 29) which is column decoder output must be Vdd for 22,23,24 pins connected to Vss otherwise it should be low.

11. Testing photodiode: Project LED onto chip and observe output current at pin 9

12. Project LED of frequency 10kHz and check output at pin Vph(pin 11) which is input of the high pass filter of the test pixel.

13. Connect pin 26(Vswitch) to Vdd and check output at pin 10(Vhpf)

14. Check output at pin 33(Vsquare) which is the output of comparator and it should be square wave of frequency 10kHz.

15. Check output at pin 32(Vedge) which is the output of edge detector of the test pixel.

16. Check output bits at pin 37(op7), pin 38(op6), pin 39(op5), pin 40(op4), pin 1(op3), pin 2(op2), pin 3(op1), pin 4(op0).
REFERENCES


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