REVERSE NESTED MILLER COMPENSATION USING CURRENT BUFFERS IN A THREE STAGE LOW DROP-OUT VOLTAGE REGULATOR

BY

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ABSTRACT

REVERSE NESTED MILLER COMPENSATION USING CURRENT BUFFERS IN A THREE STAGE LOW DROP-OUT VOLTAGE REGULATOR

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In this work we present a novel frequency compensation scheme, Reverse Nested Miller Compensation using Current Buffers (RNMCCB), for multi-stage amplifiers.

As opposed to previous reverse nested schemes, our work uses inverting gain stages for both the second and third stages. The outer compensation loop utilizes a current mirror as an inverting current buffer (CB) and the inner-loop uses a common-gate amplifier as a CB, creating two left-half-plane (LHP) zeros. We introduce a simple and effective method of placing a resistor in series with a CB for
accurate placement of LHP zeros. As a design example of the RNMCCB scheme, we propose a three-stage low drop-out voltage regulator (LDO) in a 0.5µm CMOS process to supply 1.21V to a load ranging from 1µA to 100mA. Our design goals were to simultaneously achieve very high current efficiency and very low transient output voltage variation. As such, we achieved a 99.95% current efficiency and a maximum load transient output voltage variation of ±48mV with an output capacitor of 100nF. Experimental results, in good agreement with theoretical analysis, validate the novel RNMCCB frequency compensation scheme.

Also we discuss an essential modification to a conventional four-stage pseudo-class AB amplifier resulting in a true class AB amplifier. As opposed to the conventional pseudo-class AB scheme, which uses a current mirror in the third stage, our work uses an adaptive biasing circuit in the third stage in order to drastically reduce quiescent current. The pseudo-class AB and new class AB amplifiers are designed in a 0.5µm process with power supplies of ±1.5V for a phase margin of 67° while driving a load of 32Ω∥500pF.
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1 INTRODUCTION

As dimensions of transistors become smaller, the supply voltage is getting lower, and the gain of each transistor is getting smaller. For achieving high gain, multistage amplifiers are implemented. In order to stabilize multistage amplifiers negative feedback is utilized. To this end the reverse nested Miller compensation using current buffers (RNMCCB) network is proposed.

In Chapter 2, it is mentioned that Reversed nested Miller compensation (RNMC) is a preferred candidate for multistage amplifiers as it provides improvement in small-signal and large signal amplifier characteristics, such as increased bandwidth and reduced settling time. Compared to nested Miller compensation (NMC), the inner compensation capacitor in RNMC does not load the output. RNMC is especially suited to drive heavy capacitive loads [GPP07]. In previous work, three-stage amplifiers employing NMC required a second stage that is non-inverting [YESS97, LM01b, LM01a, PP02a, LM03, PS04a, PS04b] and those employing RNMC required a third stage that is non-inverting [GPP07, MPP03, ZYHSS05, SHH06, JYR08, MPP09]. In [GPP07, YESS97, LM01b, LM01a, LM03, PS04a, PS04b, MPP03, ZYHSS05, SHH06, JYR08, MPP09] the low-voltage non-inverting stage is realized using a common-source amplifier with an output mirror, as shown in Fig. 1.

In [PP02a], a second differential amplifier forms the non-inverting stage. If
Figure 1: Typical implementation of third gain stage in a RNMC topology, adapted from [GPP07]

the non-inverting stage of Fig. 1 were replaced with an inverting stage, a simpler common-source amplifier could be used, thereby eliminating the quiescent current in one branch, as well as the corresponding transistors.

To this end, the reverse nested Miller compensation using current buffers (RN-MCCB) network is proposed, as shown in Fig. 2. Current Buffers (CBs), in combination with series compensation capacitors $C_{C1}$ and $C_{C2}$, produce two Left-Half-Plane (LHP) zeros, which cancel one of the system non-dominant poles, resulting in improved stability.
Figure 2: Proposed reverse nested Miller compensation using current buffers.

1.1 RNMCCB Compensation Scheme

In contrast to previously implemented NMC and RNMC schemes, we introduce a new topology in the compensation network wherein both the second and third stages can be inverting. It is precisely the inverting CB in the outer feedback loop that allows the two latter stages to both be inverting. The proposed RNMCCB network doesn’t require any additional active components, thereby introducing no additional static power consumption. An additional series resistor in the CB feedback loop allows for accurate placement of the LHP zero. Simple design equations, accurately predicting the loop-gain, pole-zero locations and phase margin are developed. This work has been reported in [GRF10].
1.2 LDO Implementation with Improved Transient Response

Low drop-out voltage regulators (LDOs) are an indispensable part of today’s high performance System-on-Chip [HKS’08] and Power Management ICs [SWZ’07], because of their ease of integration, low noise, high PSRR and low quiescent current. RNMCCB utilization in three-stage low drop-out voltage regulator (LDO) resulted in a low quiescent current architecture with very tight transient response. We demonstrate two degrees of freedom in choosing the location of the LHP zeros in the LDO design.

1.3 Compensation Network Using Current Buffers

Fig. 3(a) shows traditional Miller compensation, used to split the poles associated with the nodes X and Y. In addition to pole splitting, the Miller capacitor $C_m$ forms a feedforward path [GM82, HLK’04] resulting in a Right-Half-Plane (RHP) zero. This RHP zero is moved to the LHP, by choosing an appropriate value for the nulling resistor $R_m$ as in Fig. 3 (b).

On the other hand, CBs obviate the feedforward path and introduce LHP zeros, improving PM, stability and gain-bandwidth. Fig. 3 (c) shows the current mirror as a CB [HLK’04, RM00, LML07] with compensation capacitor $C_{C1}$, introducing a LHP zero at $g_{mBU}/C_{C1}$. The current mirror forms an inverting CB. Fig. 3(d) shows a common-gate amplifier with compensation capacitor $C_{C2}$, referred to as cascode compensation [GM82, Ahu83]. This network introduces a LHP zero at
Figure 3: Cancelation techniques for Miller RHP zero: (a) Miller compensation (b) Miller compensation with nulling resistor (c) Inverting current buffer compensation (d) Ahuja cascode compensation (e) Resistor $R_{C1}$ in series with inverting current buffer (f) Modified cascode compensation. The approximate equations for the RHP and LHP zeros are also given.
\( g_{mCG}/C_2 \) and is utilized in [GPP07, PS04b, MPP03, SHH06, JYR08, MPP09, HKB+05, ASLP07]. A resistor \( R_{Ci} \) can be placed in series with the BU and compensation capacitor \( C_{Ci} \), as shown in Figs. 3 (e). The new location of the LHP zero is given by

\[
\omega_{Z, CB} = \frac{1}{C_1(1/gmBU + R_{C1})} \approx \frac{1}{R_{C1}C_1} \tag{1}
\]

Also a resistor \( R_{C2} \) can be placed in series with the common gate amplifier (CG) and compensation capacitor \( C_{C2} \), as shown in Figs. 3 (f). The new location of the LHP zero is given by

\[
\omega_{Z, CB} = \frac{1}{C_2(1/gmCG + R_{C2})} \approx \frac{1}{R_{C2}C_2} \tag{2}
\]

The thesis is organized as follows. Previously reported compensation networks are reviewed in Chapter 2. The proposed RNMCCB design, implementation and analysis of the LDO are presented in Chapter 3, followed by experimental results in Chapter 4. A simple but effective scheme for converting a pseudo-class AB amplifier to a true class AB amplifier is introduced in Chapter 5. Conclusions appear in Chapter 6.
2 Feedback Amplifier Networks

Feedback network is necessary in almost all electronic circuits and systems. Feedback describes the situation when a fraction of the output signal is used to modify the effective input signal. If the feedback signal has a relative phase angle that decreases the effective magnitude of the input signal of the system, the feedback is said to be negative or degenerative, and the system will tend to be stable. Because negative feedback tends to produce stable circuit responses, it is used in most circuit and system design [PP02b]. If the signal increases the effective magnitude of the input signal of the system then it is called positive or regenerative.

2.1 Previously Reported Feedback Networks

In this section we review the previously reported feedback networks

2.1.1 Single Miller Compensation (SMC)

Single Miller Compensation is discussed in many articles and textbooks [PP02b, SS95, Bak07, Raz00, Raz06, EH95, LM01a]. By putting a compensation capacitor between the input and output nodes an of inverting stage, a SMC network is formed. The dominant pole is created due to Miller feedback. Fig. 4 shows the SMC structure.
Assuming $C_L$ is not large. The dominant $p_{-3db}$ pole is $1/(C_m g_{m2} R_1 R_L)$. The nondominant is $g_{m2}/C_L$. As the gain of the second stage $g_{m2}$ increases, the dominant pole shifts more towards the origin and the nondominant pole shifts away from the origin. In this way, pole splitting takes place and the amplifier is stabilized but at reduced bandwidth. Also the Miller capacitor creates a high frequency feedforward path. This path creates a right half path (RHP) zero which reduces stability. The RHP zero $z_1$ is located at $1/g_{m2} C_L$. 

Figure 4: Single Miller Compensation
2.1.2 Single Miller Compensation Network with Nulling Resistor (SM-CNR)

To nullify the RHP zero due to the feedforward path through the Miller capacitor, a nulling resistor is placed in series with the compensation capacitor (SMCNR). This technique of adding a series nulling resistor is discussed in many articles and textbooks [PP02b, SS95, Bak07, Raz00, Raz06, EH95, LM01a]. Fig. 5 shows the SMCNR structure.

![Diagram of Single Miller Compensation with Nulling Resistor](image)

Figure 5: Single Miller Compensation with Nulling Resistor

Again assuming $C_L$ is not large the dominant $p_{-3db}$ pole is $1/(C_m(R_m+g_{m2}R_1R_L))$, the nondominant pole is $(R_m+g_{m2}R_1R_L)/(C_L(R_1+R_m)R_L)$, and the RHP zero $z_1$ is $1/(R_m-1/g_{m2})C_m$. So by choosing $R_m = 1/g_{m2}$ the RHP zero can be eliminated [LM01a, Bak07, Raz00].
2.1.3 Single Miller Compensation Network with Multipath Zero Cancellation (SMCMZC)

Single Miller Compensation Network with Multipath Zero Cancellation (SMCMZC) is shown in Fig. 6. This technique is reported in [EH95]. This technique does not require any additional circuity to cancel the RHP zero and the position of the poles are not effected.

As shown in Fig. 6 the feedforward path adds a current to the feedforward current and cancels the RHP zero. The dominant $p_{-3db}$ pole is $1/(C_m g_{m2} R_1 R_L)$, the nondominant pole is $g_{m2}/C_L$, and the zero $z_1$ is $g_{m1} g_{m2}/C_m (g_{mf} - g_{m1})$. If $g_{mf} = g_{m1}$ the RHP is totally canceled.
2.1.4 Nested Miller Compensation (NMC)

As the dimensions of transistors become smaller, the inherent gain of each amplifier stage is reducing. In order to achieve high gain, multistage amplifiers are required. Multistage amplifiers have poles associated with each stage. Achieving stability is more complicated than for single stage op amps. To achieve stability for multistage amplifiers Nested Miller Compensation (NMC) was proposed [LM01a, EH95, PP02b, EKH92]. NMC is an extension of version of SMC. Fig. 7 shows the structure of three stage Nested Miller Compensation. The Transfer function of the circuit shown in Fig. 7 is adopted from [LM01a] and given by:

![Nested Miller Compensation Diagram](image-url)

Figure 7: Nested Miller Compensation

function of the circuit shown in Fig. 7 is adopted from [LM01a] and given by:
\[ A_{nmc} = \frac{g_{m1}g_{m2}g_{m3}R_1 R_2 R_L (1 - s \frac{C_{m2}}{g_{m3}} - s^2 \frac{C_{m1}C_{m2}}{g_{m2}g_{m3}})}{(1 + sC_{m1}g_{m2}g_{m3}R_1 R_2 R_L) (1 + s \frac{C_{m2}(g_{m3} - g_{m2})}{g_{m2}g_{m3}} + s^2 \frac{C_{m2}C_{mL}}{g_{m2}g_{m3}})} \]  

(3)

The dominant \( p_{-3db} \) pole is \( 1/(C_{m1}g_{m2}g_{m3}R_1 R_2 R_L) \). The second and third poles are the roots of second order polynomial in the denominator of (3). From the numerator of (3) we can see there are two RHP zeros. The Gain Bandwidth (GBW) is given by \( g_{m1}/C_{m1} \) or \( 1/4(g_{m3}/C_L) \).

### 2.1.5 Nested Miller Compensation with Nulling Resistor (NMCNR)

NMCNR was first proposed in [LMK99]. Fig. 8 shows the structure of a three stage Nested Miller Compensation with Nulling Resistor. Here a resistor is added in series to the compensation capacitances in order to eliminate the RHP zeros.

The transfer function of the circuit shown in Fig. 8 is adopted from [LM01a] and given by:

\[ A_{nmcnr} = \frac{g_{m1}g_{m2}g_{m3}R_1 R_2 R_L (1 - s \left[ C_{m1}R_m + C_{m2}(R_m - \frac{1}{g_{m3}}) \right] - s^2 \frac{C_{m1}C_{m2}(g_{m3}R_m - 1)}{g_{m2}g_{m3}})}{(1 + sC_{m1}g_{m2}g_{m3}R_1 R_2 R_L) (1 + s \frac{C_{m2}(g_{m3} - g_{m2})}{g_{m2}g_{m3}} + s^2 \frac{(1-g_{m2}R_m)C_{m2}C_{mL}}{g_{m2}g_{m3}})} \]  

(4)

From (4) we can see by choosing \( R_m \geq \frac{1}{g_{m3}} \) the effect of the RHP zeros can be nullified or shifted to the left half plain (LHP) [LM01a].
2.1.6 Multi-path Nested Miller Compensation (MNMC)

In this topology, a feedforward stage is added from the input to the intermediate node of the amplifier[EKH92, EH95, LM01a]. Multi-path Nested Miller Compensation (MNMC) is shown in Fig. 9. The feedforward path provides a left half-plane (LHP) zero which cancels the effect of the second non-dominant pole to increase the gain-bandwidth. This technique requires additional circuitry and power consumption.

2.1.7 Nested Miller Compensation with Feedforward Path (NMCF)

In this topology, a feedforward stage is added from the intermediate node to the output node of the amplifier[LM01a]. The difference between MNMC and
NMCF is that the feedforward stage is not connected from the input but from the intermediate stage and $g_{mf1} \geq g_{m2}$. Nested Miller Compensation with Feedforward path is shown in Fig. 10.

2.1.8 Nested Transconductance Capacitance Compensation (NGCC)

NGCC was first proposed in [YESS97]. The difference between NGCC and NMCF is that in NGCC a total of $N-1$ nested feedforward transconductance stages are required for an $N$ stage amplifier, as shown in Fig. 11. Compared to NMCF, NGCC has simpler stability conditions since each feedforward path introduces a LHP zero which improves the overall frequency response. On the other hand, circuit complexity and power consumption is much more in NGCC than NMCF.
Figure 10: Nested Miller Compensation with Feedforward Path

and MNMC.

2.1.9 Nested Miller Compensation with Feedforward Transconductance stage and Nulling Resistor (NMCFNR)

This topology uses one feedforward path from the output of the first stage to the output of the amplifier in order to eliminate the high frequency RHP zero due the $C_{m2}$. Also the nulling resistor $R_m$ is used to further eliminate the RHP zeros. This topology was introduced in [LM01b]. The topology of NMCFNR is shown in Fig. 12.
2.1.10 Damping-Factor-Control Frequency Compensation (DFCFC)

All of the Nested Miller Compensation technique suffer from low Gain Bandwidth (GBW) mainly because of the presence of $C_{m2}$. But $C_{m2}$ is required mainly to control the damping factor of the non-dominant poles [LMKS00b, LM01a]. Removing $C_{m2}$ and adding a damping factor controller block is an option. The damping factor controller block requires additional circuits and power but, on the other hand, provides much higher GBW. Damping-Factor-Control Frequency Compensation was first reported in [LMKS00b, LMS99]. Damping-Factor-Control Frequency Compensation 1 (DFCFC1) is shown in Fig. 13.

An alternative version of Damping-Factor-Control Frequency Compensation 2 (DFCFC2) was reported in [LMKS00a]. The topology of Damping-Factor-Control...
2.1.11 Active Feedback Frequency Compensation (AFFC)

This topology was introduced in [LM04]. The topology is show in Fig. 15. This structure has an input stage, a high gain block (HGB) and a high speed block (HSB). The HSB has one feedforward path through $g_{mf}$ and one feedback path through $g_{ma}$ and $C_{m2}$. Also it has one compensation capacitor $C_{m1}$ from the output of the second stage to the output of the amplifier. The dominant $p_{-3db}$ pole is $1/(C_{m1}g_{m2}g_{m3}R_1R_2R_L)$. Also there are two nondominant poles and one LHP zero $g_{ma}/C_{m2}$ in this configuration.
2.1.12 Reversed Nested Miller Compensation (RNMC)

As mentioned earlier, NMC suffers from low GBW. The GBW of NMC is inversely proportional to the load capacitance. This make NMC unable to drive large load capacitances. In order to over come NMC’s drowback RNMC was proposed. For a three stage amplifier in witch the second is the only inverting one, the most suitable option is reversed nested Miller compensation RNMC [EH95, PP02b]. The topology of Reversed Nested Miller Compensation (RNMC) is shown in Fig. 16.

The transfer function of the circuit shown in Fig. 16 is adapted from [PP02b]
and given by:

\[
A_{\text{rnmc}} = \frac{g_{m1}g_{m2}g_{m3}R_1R_2R_L(1 - s(C_{m2}/g_{m2} + C_{m1}/g_{m2}g_{m3}R_2) - s^2C_{m1}C_{m2})}{(1 + s(C_{m1}g_{m2}g_{m3}R_1R_2R_L))(1 + s(C_{m2}C_{m3}/g_{m2} + C_{m2}/g_{m3} + s^2C_{m1}C_{m3})))}
\]  

(5)

The dominant \(p-3db\) pole is \(1/(C_{m1}g_{m2}g_{m3}R_1R_2R_L)\). Equation (5) has two higher frequency poles and two RHP zeros.

2.1.13 Reversed Nested Miller Compensation with Nulling Resistor (RNMCNR)

In order to eliminate the RHP zeros, a resistor is added in series with the compensation capacitances [MPP03]. Fig. 17 shows the structure of a three stage Reversed Nested Miller Compensation with Nulling Resistor.
2.1.14 Reversed Nested Miller Compensation with Voltage Follower (RNMCVF)

This topology uses one voltage follower in the inner loop [DCMPP02] to send the RHP zero to a very high frequency. Fig. 19 shows the structure of a three-stage amplifier with Reversed Nested Miller Compensation with Voltage Follower. Using the voltage follower shifts the RHP zero on RNMC to very high frequency, since it gets multiplied by $g_{m2}R_2$. 

![Diagram](image.png)

Figure 15: Active Feedback Frequency Compensation
2.1.15 Reversed Nested Miller Compensation with Voltage Follower & Nulling Resistor (RNMVFNFR)

This topology uses both a voltage follower in the inner loop and a nulling resistor to block the feedforward path [HCCP03]. Fig. 19 shows the structure of a three stage Reversed Nested Miller Compensation with Voltage Follower & Nulling Resistor. The nulling resistor helps improve the phase margin.

2.1.16 Reversed Nested Miller Compensation with Current Follower (RNMCCF)

Fig. 20 shows the structure of a three stage Reversed Nested Miller Compensation with Current Follower. Reversed Nested Miller Compensation with Current
Figure 17: Reversed Nested Miller Compensation with Nulling Resistor

Figure 18: Reversed Nested Miller Compensation with Voltage Follower
Figure 19: Reversed Nested Miller Compensation with Voltage Follower & Nulling Resistor

Figure 20: Reversed Nested Miller Compensation with Current Follower
Follower Compensation was reported in [MPP03]. In order to eliminate the two RHP zeros of (5) the current follower is used.

2.1.17 Reversed Nested Miller Compensation with Voltage Buffer and Outer Resistor (RNMC-VB-OR)

This is a improved version of RNMCVF. This topology was proposed in [GMPP07]. The topology of Reversed Nested Miller Compensation with Voltage Buffer and Outer Resistor $R_m$ is shown in Fig. 21. The presence of the resistor and feedforward path gives better phase margin than RNMCVF and RNMCVFNR.

![Reversed Nested Miller Compensation with Voltage Buffer and Outer Resistor](image)

Figure 21: Reversed Nested Miller Compensation with Voltage Buffer and Outer Resistor
2.1.18 Nested Feedforward Reversed Nested Miller Compensation (NFRNMC)

The topology of NFRNMC is shown in Fig. 22. This structure was introduced in [ZYHSS05]. Here, two feedforward paths, one \( g_{m_f1} \) from input to output and the other \( g_{m_f2} \) from the output of stage 1 to output, are added to the conventional RNMC structure. The additional of the feedforward paths completely eliminate the RHP zeros of equation (5).

![Figure 22: Nested Feedforward Reversed Nested Miller Compensation](image)

2.1.19 Crossed Feedforward Reversed Nested Miller Compensation (CFRNMC)

This structure was also proposed in [ZYHSS05]. Here the first feedforward path \( (g_{m_f1}) \) is connected from input to output of the second output stage but the
second feedforward path \((g_{mf2})\) remains the same as NFRNMC. The change in
the first feedforward path gives a LHP zero which gives better phase margin. The
CFRNMC topology is shown in Fig. 23.

![Crossed Feedforward Reversed Nested Miller Compensation](image)

**Figure 23: Crossed Feedforward Reversed Nested Miller Compensation**

### 2.1.20 Reversed Nested Miller Compensation with Feedforward &
Nulling Resistor (RNMCFNR)

This compensation scheme has the reversed version of NMCFNR [GPP07]. This
structure was reported in [GPP07]. Because of its reverse nested configuration,
it has much higher GBW and is able to drive much larger load capacitor than
NMCFNR with smaller \(C_m1\) and \(C_m2\). The topology of RNMCFNR is shown in
Fig. 24.
2.1.21 Reversed Active Feedback Frequency Compensation (RAFFC)

This structure was also proposed in [GPP07]. This structure uses a current buffer in the outer loop. This compensation scheme is the reversed version of AFFC shown in [LM04]. The topology of RAFFC is shown in Fig. 25.
Figure 25: Reversed Active Feedback Frequency Compensation
3 Reversed Nested Miller Compensation using Current Buffer

In this chapter we discuss the proposed Reversed Nested Miller Compensation using Current Buffer (RNMCCB).

3.1 Proposed Reversed Nested Miller Compensation using Current Buffer Scheme

A generic three-stage amplifier RNMCCB topology is shown in Fig. 2. The transconductance, output resistance and lumped parasitic capacitance of \(i\)th stage are represented by \(g_{mi}, R_i\) and \(C_i\) respectively. Assuming that the \(C_i\)'s \(\ll C_{C1}, C_{C2},\) and \(C_L\), and the poles are widely separated, small-signal analysis yields the transfer function given in :

\[
A_{RNMCCB} \approx A_{DC} \left(1 + \frac{s}{\omega P_1}\right) \left(1 + \frac{s}{C_{C2} g_{mBU}} \right) \left(1 + \frac{s}{C_{C1} g_{mBU}} \right) \left(1 + \frac{s^2 C_{C2} C_L}{g_{mBU} g_{m3}} \right)
\]

\[= A_{DC} \left(1 + \frac{s}{\omega P_1}\right) \left(1 + \frac{s}{C_{C2} g_{mCG}} \right) \left(1 + \frac{s}{C_{C1} g_{mBU}} \right) \left(1 + \frac{s}{g_{m3} C_{C1}} \right) \left(1 + \frac{s}{g_{mBU}} \right)
\]

(6)

The dc voltage gain is given by

\[A_{DC} = g_{m1} R_1 g_{m2} R_2 g_{m3} R_3\]

(7)

The dominant pole is given by

\[
\omega P_1 = \frac{1}{R_1 C_{C1} g_{m2} R_2 g_{m3} R_3}
\]

(8)
and the LHP are is given by

\[\omega_{Z1} = -\frac{g_{mBU}}{C_{C1}} \]

(9)

\[\omega_{Z2} = -\frac{g_{mCG}}{C_{C2}} \]

(10)

The gain-bandwidth product \(\omega_{GBW}\) is approximated as

\[\omega_{GBW} \approx g_{m1} C_{C1} \]

(11)

Then the phase margin (PM) can be expressed as

\[PM = 90^\circ - \tan^{-1}\left(\frac{\omega_{GBW}}{\omega_{P2}}\right) + \tan^{-1}\left(\frac{\omega_{GBW}}{\omega_{Z2}}\right)\]

\[\approx \tan^{-1}\left[\frac{g_{m1}^2 C_{C2}^2 C_L + g_{mCG} g_{m3} C_{C1}^3}{g_{m1} C_{C1} C_{C2} (g_{mCG} C_L - g_{m3} C_{C1})}\right] \]

(12)

If \(C_L \gg C_{C1}, C_{C2}\), PM approximates to \(\tan^{-1}\left(\frac{\omega_{GBW}}{\omega_{Z2}}\right)\) and the placement of \(\omega_{Z2}\) determines the phase margin.

### 3.2 CIRCUIT DESIGN AND IMPLEMENTATION OF LDO

Fig. 26 shows the proposed LDO. The error amplifier is realized by a folded-cascode amplifier \((M_1 - M_{11})\). Transistor \(M_{12}\) realizes a common-source gain stage (stage 2) with an adaptive load. The third stage is the power stage. Small-valued capacitors \(C_{f1}\) and \(C_{f2}\) are placed in parallel with sampling resistors \(R_{f1}\) and \(R_{f2}\), respectively, in order to filter high frequency noise and improve high frequency performance [WE06]. \(C_{OUT}\) is the off-chip output capacitor.
From Fig. 26, the output resistance of the first and third stages are given by:

\[ R_1 = \left[ r_{o11}g_{m9}r_{o9} || g_mCGr_{o7}(r_{o5} || r_{o2}) \right] \]  \hspace{1cm} (13)

\[ R_3 = \left[ r_{oP} \right] (R_{f1} + R_{f2}). \]  \hspace{1cm} (14)

The adaptive load of stage 2 consists of a diode-connected transistor \( M_{13} \) and resistors \( R_{ad1} \) and \( R_{ad2} \). At very low output currents, transistor \( M_{13} \) is in cutoff and the stage 2 load is simply \( R_{ad2} \). At higher output currents, \( M_{13} \) goes into saturation and the second stage output resistance becomes

\[ R_2 = \left( \frac{1}{g_{m13}} + R_{ad1} \right) \left| R_{ad2} \right. \]  \hspace{1cm} (15)

Figure 26: Schematic of the three-stage low drop-out voltage regulator compensated using reverse nested Miller compensation using current buffers.
The effect of this adaptive load is what is known as pole tracking, which is an effective means of improving the gain and phase margins while operating at reduced bias currents [WE06, LZC08]. At low load currents, the quiescent current in stage 2 is designed to be low. As the load current increases, the quiescent current increases, moving the non-dominant pole at the output of stage 2 to higher frequencies as $\frac{1}{g_{m13}}$ is reduced. The LDO uses the RNMCCB compensation network, with the following additional components:

- Resistor $R_{C2}$ in series with capacitor $C_{C2}$ in the inner loop. $R_{C2}$ helps shifting the CB LHP zero towards the origin.

- Miller capacitor $C_m$ with nulling resistor $R_m$ in parallel with the cascode compensation network, to effectively add another pole-zero pair to the inner loop.

The motivation for using the modified RNMCCB network is to have enhanced flexibility in minimizing under-shoot and over-shoot in the transient response of the LDO.

The AC model shown in Fig. 27 is used to conduct a detailed pole-zero analysis with and without RNMCCB. The DC loop-gain of the LDO is given by

$$A_{DC-LDO} = \beta g_{m1} R_1 g_{m2} R_2 g_{mP} R_{out}.$$ (16)
Figure 27: Small signal diagram of RNMCCB scheme implemented in the LDO.

where $\beta$ is the feedback factor. LDO-specific assumptions are: $C_{gs}$ ($C_2$ in Fig. 2) and $C_{gd}$ of the pass transistor are comparable to $C_{c1}$ and $C_{c2}$, $C_{OUT}$ is dominant, and $g_{mp}$ ($g_{m3}$ in Fig. 2) is very large at high load currents.

Fig. 28 illustrates the pole-zero locations (a) with no compensation, and (b) with RNMCCB. Prior to compensation, three relatively closely-spaced poles exist. After compensation, these poles are effectively split. The compensation network introduces three new zeros and three new poles. The dominant pole and zero of the proposed LDO are set by capacitor $C_{C1}$ with current mirror $g_{mBU}$.

Referring to Fig. 27, and assuming the zeros of the system are widely sepa-
rated, the dominant LHP zero is given by

$$\omega_{Z1} = \frac{g_{mBU}}{C_{C1}}. \quad (17)$$

Two more LHP zeros result from a combination of the cascode and Miller compensation networks, as in

$$\omega_{Z2} \approx \frac{1}{R_{C2}C_{C2} + R_mC_m} \quad (18)$$

$$\omega_{Z3} \approx \frac{1}{R_{C2}C_{C2}} + \frac{1}{R_mC_m} \quad (19)$$
The choice of $R_{C2}$, $C_{C2}$ and $R_m$, $C_m$ gives two degrees of freedom in selecting the location of the LHP zeros, as $\omega_{Z2}$ is the reciprocal of the sum of two time constants, whereas $\omega_{Z3}$ is the sum of the reciprocals of two time constants.

Two very high-frequency RHP zeros are neglected. The first occurs at the output of the first gain stage,

$$\omega_{Z4} \approx \frac{g_mCGg_{m2}R_{C2}}{C_1}, \quad (20)$$

and the second is due to $C_{gd}$ of the pass transistor $M_P$,

$$\omega_{Z5} \approx \frac{g_{mp}}{C_{gd}}, \quad (21)$$

Assuming that the first two poles of the system described by Fig. 27 are widely separated, the dominant pole of the system occurs at the output of the first stage and is given by

$$\omega_{P1} \approx -\frac{1}{R_1C_{1}g_{m2}R_2g_{mP}R_3}, \quad (22)$$

A second pole, due to the combination of Miller and cascode compensation networks, is found to be at

$$\omega_{P2} \approx -\left[R_{C2}C_{C2} + R_mC_m + \frac{C_{C2}}{g_mCG} + \frac{C_{C2}C_{OUT}}{C_{C1}g_{mP}}\right]^{-1}. \quad (23)$$
From 18 and 23, we see that $\omega_{Z_2}$ and $\omega_{P_2}$ approximately cancel each other. The third through sixth poles appear to consist of two non-dominant complex pole pairs that occur at frequencies much higher than $\omega_{GBW}$. The PM of the LDO can be calculated from

$$PM = 90^\circ - \tan^{-1}\left(\frac{\omega_{GBW}}{\omega_{P_2}}\right) + \sum_{i=1}^{3} \tan^{-1}\left(\frac{\omega_{GBW}}{\omega_{Z_i}}\right)$$

$$-\tan^{-1}\left[\frac{\omega_{GBW}}{Q\left(1 - \left(\frac{\omega_{GBW}}{\omega_{P_{3,4}}}\right)\right)}\right] - \tan^{-1}\left[\frac{\omega_{GBW}}{Q\left(1 - \left(\frac{\omega_{GBW}}{\omega_{P_{5,6}}}\right)\right)}\right]$$

(24)

The non-dominant complex pole pairs give rise to minor magnitude peaking [LML07, MMC07], due to $Q_1$ and $Q_2$ in 24. However, the effect of $Q_1$ and $Q_2$ on PM is mitigated by $\omega_{Z_3}$.

### 3.3 Biasing Circuit of RNMCCB LDO

The biasing voltages $V_{b1}, V_{b2}, V_{b3}, V_{b4}$ of Fig. 26 were generated by circuit shown in Fig. 29. This circuit was adopted from [AH02].
3.4 RNMCCB LDO Simulation

The proposed LDO shown in Fig. 26 was simulated in 0.5µm 2P3M CMOS ON Semi process with HSPICE using device dimensions given in Table 1 and Table 2.

3.4.1 RNMCCB LDO AC Testbench and AC Simulation Results

Fig. 30 shows the schematic of the AC open-loop testbench. The feedback loop from $V'_{FB}$ to $V_{FB}$ was broken and a 1GΩ was inserted. Also a 1F capacitor was placed between terminal $V_{FB}$ to ground. A resistor of value 600kΩ was connected from VDD to $I_{BIAS}$ terminal to ensure 2.2µA current.
Table 1: Device dimensions in $\mu$ of the LDO shown in Fig. 26

<table>
<thead>
<tr>
<th>Devices</th>
<th>Value($\mu/\mu$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$M_1, M_2$</td>
<td>(5.4/0.9)x16</td>
</tr>
<tr>
<td>$M_3$</td>
<td>(5.4/1.2)x8</td>
</tr>
<tr>
<td>$M_8, M_9, M_{10}, M_{11}$</td>
<td>(5.4/1.2)x4</td>
</tr>
<tr>
<td>$M_{12}$</td>
<td>(5.4/0.9)x2</td>
</tr>
<tr>
<td>$M_4, M_5$</td>
<td>(5.4/1.2)x8</td>
</tr>
<tr>
<td>$M_6, M_7$</td>
<td>(5.4/1.2)x4</td>
</tr>
<tr>
<td>$M_{13}$</td>
<td>(5.4/0.9)x4</td>
</tr>
<tr>
<td>$M_P$</td>
<td>(70.05/0.6)x360</td>
</tr>
<tr>
<td>$C_{C1}$, $R_{C2}$, $C_{C2}$</td>
<td>60pF, 20k$\Omega$, 5pF</td>
</tr>
<tr>
<td>$R_m, C_m$</td>
<td>140k$\Omega$, 200fF</td>
</tr>
<tr>
<td>$R_{f1}$, $R_{f2}$, $\beta$</td>
<td>20k$\Omega$, 200k$\Omega$, 0.909</td>
</tr>
<tr>
<td>$C_{f1}$, $C_{f2}$</td>
<td>1pF</td>
</tr>
<tr>
<td>$C_{OUT}$</td>
<td>100nF (off-chip)</td>
</tr>
</tbody>
</table>

Table 2: Device dimensions in $\mu$ of the Biasing circuit shown in Fig. 29

<table>
<thead>
<tr>
<th>Devices</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$M_{1B}, M_{2B}, M_{3B}, M_{4B}$</td>
<td>(5.4/1.2)x2</td>
</tr>
<tr>
<td>$M_{5B}, M_{6B}$</td>
<td>(5.4/1.2)x2</td>
</tr>
<tr>
<td>$R_{BIAS1}$, $R_{BIAS2}$, $I_{BIAS}$</td>
<td>250k$\Omega$, 2.2$\mu$A</td>
</tr>
</tbody>
</table>
The LDO was simulated for Load current $I_{LOAD}$ of 1µA and 100mA. Fig. 31 shows the gain and phase plots of the open-loop analysis at $I_{LOAD}$ equal for both 1µA and 100mA. For $I_{LOAD}=1$µA, $R_{LOAD}=1.21\,\text{MΩ}$ was used where as for $I_{LOAD}=1$mA, $R_{LOAD}=12.1\,\text{Ω}$ was used.

AC parameters of the LDO is given in Table 3. The parameters from Table 3 were used to calculate theoretical pole and zero locations. These calculated pole-zero locations are indicated in Fig. 32.

Fig. 33 plots PM as a function of output current. PM remains between 113°C and 117°C over the entire output current range. The simulated variation in PM is from 102° to 123° over −40°C to 80°C and $V_{LINE}$ from 1.4V to 4.2V.
### Table 3: AC CIRCUIT CHARACTERISTICS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value @ $I_{LOAD} = 1\mu A$</th>
<th>Value @ $I_{LOAD} = 100mA$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pass transistor $g_{mP}$</td>
<td>145$\mu A$/V</td>
<td>554mA/V</td>
</tr>
<tr>
<td>$g_{m1}R_1$</td>
<td>$\approx 67, dB$</td>
<td>$\approx 67, dB$</td>
</tr>
<tr>
<td>$g_{m2}R_2$</td>
<td>$\approx 16, dB$</td>
<td>$\approx 7.6, dB$</td>
</tr>
<tr>
<td>$g_{mP}R_3$</td>
<td>$\approx 27, dB$</td>
<td>$\approx 12.7, dB$</td>
</tr>
</tbody>
</table>

![Figure 32: loop gain and phase response of the three-stage LDO at $I_{LOAD} = 100mA$, $T = 27^\circ C$ with theoretical pole and zero locations indicated.](image)

Figure 32: loop gain and phase response of the three-stage LDO at $I_{LOAD} = 100mA$, $T = 27^\circ C$ with theoretical pole and zero locations indicated.
Figure 33: Phase margin versus $I_{LOAD}$ at $V_{LINE} = 2.0V$ and $T = 27^\circ C$.

3.5  RNMCCB LDO Transient Simulation

3.5.1  Load Transient Simulation

The load transient simulation testbench is shown in Fig. 34. The output current changes from $1\mu A$ to $100mA$ in $1\mu s$. Overshoot and undershoot were carefully minimized by choosing a moderate value for $C_{C2}$ (5pF) and a low value for $C_m$ (200fF). Resistor $R_m$ is needed for stability, whereas the unconventional addition of resistor $R_{C2}$ helps reduce the overshoot and undershoot to the simulated values.
Figure 34: RNMCCB LDO Load Transient Simulation Testbench.

The load transient response is shown in Fig. 35.

3.5.2 Line Transient Simulation

The line transient simulation testbench is shown in Fig. 36. The line transient response is shown in Fig. 37. The input source voltage changes from 1.8V to 2.8V in 1µs. In this response, the effect of $R_m$ and $R_{C2}$ is minimal. The simulated values of overshoot and undershoot are ±13 mV.

The line transient response is shown in Fig. 37.
Figure 35: Load transient response of the proposed LDO.

Figure 36: RNMCCB LDO Line Transient Simulation Testbench.
3.5.3 Power Up/Down Simulation

The power up-down simulation testbench is shown in Fig. 38. The Line supply voltage was changed from 0 Volt to 5 Volts in 25ms and then 5 Volt to 0 Volt in 25ms. Fig. 39 shows the power up/down simulation waveform with $R_{LOAD}=11.1\Omega$.

The drop-out voltage was calculated from this simulation result. Drop-out voltage is the voltage difference between the Line supply voltage and Output voltage, when the output voltage is 100mV below the nominal 1.21V and supplying a load current of 100mA.

The simulated transient performance of the LDO is summarized in Table 4.
Figure 38: Power Up-Down simulation Testbench.

Figure 39: Power Up-Down simulation result of the proposed LDO.
<table>
<thead>
<tr>
<th>Process</th>
<th>0.5μm CMOS 2P 3M</th>
</tr>
</thead>
<tbody>
<tr>
<td>Threshold Voltage</td>
<td>( V_{thn}=0.73\text{V},</td>
</tr>
<tr>
<td>Line Voltage ( V_{LINE} )</td>
<td>1.41V to 4.2V</td>
</tr>
<tr>
<td>Output Voltage ( V_{OUT} )</td>
<td>1.21V</td>
</tr>
<tr>
<td>Output Current ( I_{OUT} )</td>
<td>1μA to 100mA</td>
</tr>
<tr>
<td>Dropout Voltage</td>
<td>200mV @ 100mA</td>
</tr>
<tr>
<td>Total Quiescent Current</td>
<td>24.3μA @ ( I_{OUT}=1\text{μA} ), 47.2μA @ ( I_{OUT}=100\text{mA} )</td>
</tr>
<tr>
<td>Line Regulation</td>
<td>173μV/V @ ( I_{OUT}=100\text{mA} )</td>
</tr>
<tr>
<td>Load Regulation</td>
<td>(-236\ \mu\text{V}/\text{mA} @ V_{LINE}=1.8\text{V})</td>
</tr>
<tr>
<td>Load Transient Response</td>
<td>≤ 2.72% @ ( I_{OUT}=1\text{μA} ) to 100mA in 1μs, ≤ 2.9% @ ( I_{OUT}=100\text{mA} ) to 1μA in 1μs</td>
</tr>
<tr>
<td>Line Transient Response</td>
<td>≤1.09% @( V_{LINE}=1.8\text{V} ) to 2.8V in 1μs, ≤ 1.07% @( V_{LINE}=2.8\text{V} ) to 1.8V in 1μs</td>
</tr>
<tr>
<td>Current Efficiency @ ( I_{LOAD}=100\text{mA} )</td>
<td>99.95%</td>
</tr>
</tbody>
</table>
3.6 RNMCCB LDO LAYOUT

The layout of the proposed LDO is shown in Fig. 40. The overall regulator size was 0.263 $mm^2$. The layout of the LDO was sent to MOSIS for fabrication.
4 EXPERIMENTAL RESULTS

4.1 Introduction

To verify the effectiveness of the proposed compensation scheme, the circuit of Fig. 26 was fabricated in a 0.5\(\mu\)m 2P3M CMOS process. Fig. 41 shows the micrograph of the fabricated LDO. The LDO nominal output voltage \(V_{OUT}\) is 1.21V and was designed to operate at \(I_{LOAD-MIN}\) of 1\(\mu\)A and \(I_{LOAD-MAX}\) of 100mA. The LDO has an input voltage range \(V_{LINE}\) of 1.4V to 4.2V, and a maximum current efficiency of 99.95\%, making it desirable for Li-ion battery-powered portable applications. The total measured quiescent current \(I_Q\) at \(I_{LOAD-MIN}\) is 24\(\mu\)A. It rises to 45\(\mu\)A at \(I_{LOAD-MAX}\). This change in bias current is due to the adaptive load of stage 2. Our bias current measurements include current drawn by the sampling resistors and the bias voltage generator. All the results of this work has been reported in [GRF10].

4.2 Line Transient Test

The line transient response is shown in Fig. 42. \(V_{LINE}\) changes from 2V to 3V with 100ns rise time. Overshoot is measured as +23mV. Undershoot is measured as –12mV.
Figure 41: of the proposed LDO (active area: 878µm x 300µm).

Figure 42: Measured line transient response with $C_{OUT} = 100\text{nF}$ and $I_{LOAD} =$ 1mA.
4.3 Load Transient Test

The load transient response is shown in Fig. 43. The output current changes from $1\mu A$ to 100mA with a rise time of 100ns. Overshoot and undershoot were carefully minimized by the selection of $C_{C2}$, $C_m$, $R_m$, and $R_{C2}$. The measured values are $-48mV$ and $+47mV$, respectively. The measured DC line regulation is $98\mu V/V$ at $I_{LOAD}=1mA$. The measured DC load regulation is $250\mu V/mA$. A large portion of this load regulation can be attributed to the IR drop across the bondwire. In Figs. 42 and 43, we see small-amplitude, damped high-frequency oscillations in the transient response, which we attribute to the high-frequency complex-pole pairs.
5 Adaptive Biasing Technique for Class AB Output Stage

As battery-powered circuits become ubiquitous, the demand for highly current-efficient amplifiers and drivers is increasing in order to reduce the size and/or increase the lifetime of the battery [LMBRAC05]. However, as the dimensions of transistors become smaller, the inherent gain of each transistor stage is reducing. In order to achieve high gain, multistage amplifiers are required. High current efficiency is generally achieved by employing a class AB push-pull output stage. As a result, multistage class AB amplifiers are among the most widely used circuits in battery-powered applications.

5.1 A Conventional Pseudo-Class AB Amplifier

A low-voltage [EHH94] four-stage pseudo-class AB four-stage amplifier has been widely reported in the literature [GPP07, MPP03, ZYHSS05]. Its schematic is given in Fig. 44. This pseudo-class AB amplifier requires a large amount of bias current whenever the output load current is large and positive due to the current mirror formed by transistors $M_{13} - M_{15}$ between the third and fourth stages. On the other hand, when driving a large and negative output load current, the bias current remains low. The designation pseudo-class AB results from the fact that the maximum positive output current is proportional to the bias current of the
third stage.

![Schematic of the four-stage conventional pseudo-class AB amplifier.](image)

Figure 44: Schematic of the four-stage conventional pseudo-class AB amplifier.

### 5.2 Improved Class AB Topology

To overcome the problem of a large bias current in the third stage, we are proposing an adaptive biasing circuit in the third stage, as shown in Fig. 6. This essential change converts the output stage to true class AB, such that the maximum output current is much larger than the bias current [SS95]. This adaptive biasing circuit also known as pole-tracking, finds use in low dropout voltage regulator applications [WE06, LZC08].

Referring to Fig. 6, the input stage is implemented using a folded-cascode amplifier with transistors $M_1 - M_9$. Transistors $M_{10} - M_{12}$ realize a common-
source gain stage. The third stage $M_{13} - M_{14}$ also realizes a common-source gain stage with the proposed adaptive load. The fourth stage is the push-pull output stage, formed by $M_{15} - M_{16}$.

Figure 45: Schematic of the four-stage true class-AB using adaptive biasing technique.

The third stage bias current adapts so as to boost the output load current when a large positive input signal is applied, yielding a maximum positive load current much larger than the quiescent current. The adaptive load of stage 3 consists of a diode-connected transistor $M_{13}$ and resistors $R_{ad1}$ and $R_{ad2}$. At very low output currents, transistor $M_{13}$ is in cutoff and the stage 3 load is simply $R_{ad2}$. The presence of parallel resistor $R_{ad2}$ helps move the non-dominant pole at the gate of M15 to higher frequencies and improves the overall phase margin of
the amplifier [LZC08].

At higher output currents, $M_{13}$ goes into saturation and the third stage load resistance becomes $(1/g_{m13} + R_{ad1}) \parallel R_{ad2}$. The presence of Rad1 in the source of $M_{13}$ forms an inverse-Wildar current mirror between $M_{13}$ and $M_{15}$ [Wid65]. Depending on the choice of resistor values, the output resistance of third stage of the proposed class AB amplifier can be much higher than that of the conventional pseudo-class AB amplifier, which is $1/g_{m13}$. As a result, the overall gain of the proposed class AB amplifier can be proportionally higher, as well.

5.3 Simulation Results

The circuits in Fig. 44 & Fig. 6 were simulated in 0.5µm 2P3M CMOS ON Semi process using device dimensions given in Table 5. The push-pull output stage has dimensions that are 6x to 12x that of the first three stages, so as to be able to sink and source large load currents. Compensation networks were designed for each amplifier such that a phase margin of 67° was achieved in both cases. The true class-AB amplifier required an additional Miller capacitor with nulling resistor ($R_{m1}$ and $C_{m1}$ in Fig. 6) so as to achieve the desired phase margin.

The amplifiers were configured as inverting amplifiers with a gain of negative four, driving a load of 32Ω||500pF. Fig. 46 shows transient simulation results of both the pseudo-class AB and class AB amplifiers where the input is a square wave of 100mV with rise and fall times of 10ns. At a maximum negative load
current, $I_{L_{\text{MAX}-}}$, of $-12.5\text{mA}$, both amplifiers consume $44\mu\text{A}$ of quiescent current. However, at a maximum positive load current, $I_{L_{\text{MAX}+}}$, of $+12.5\text{mA}$, the pseudo-class AB consumes $1.22\text{mA}$ of bias current. On the other hand, the true class AB amplifier consumes only $140\mu\text{A}$ for the same output load current.

A summary of bias currents at different load currents is summarized in Table 6. The current boosting factor (CBF), defined as $I_{L_{\text{MAX}}}/I_Q$ in [LMBRAC05], is 89 for the proposed amplifier, compared to a value of 10.2 for the conventional pseudo-class AB amplifier, for a positive load current of $12.5\text{mA}$.

A performance comparison of the two amplifiers is given in Table 7. The major difference between the two amplifiers is the gain, which improves from $53.7\text{ dB}$ for the pseudo-class AB amplifier to $71.9\text{ dB}$ for the class AB amplifier. As described earlier, this increase is due to the higher load resistance of stage 3.
Figure 46: Simulation results (a) Input waveform with rise and fall time of 10ns  
(b) Output waveforms with gain= - 4 (c) Load Current while driving 32Ω∥500pF  
Quiescent currents (d) VDD supply current (e) VSS supply current.
Table 5: Device dimensions in μ

<table>
<thead>
<tr>
<th>Devices</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$M_1, M_2, M_8, M_9$</td>
<td>(30/1.2)x2</td>
</tr>
<tr>
<td>$M_3, M_{14}$</td>
<td>(30/1.2)x2</td>
</tr>
<tr>
<td>$M_{12}$</td>
<td>(30/1.2)x4</td>
</tr>
<tr>
<td>$M_4, M_5, M_6, M_7, M_{10}, M_{11}, M_{13}$</td>
<td>(30/1.2)x2</td>
</tr>
<tr>
<td>$M_{15}, M_{16}$</td>
<td>(30/1.2)x24</td>
</tr>
<tr>
<td>$R_{ad1}, R_{ad2}$</td>
<td>70kΩ, 170kΩ</td>
</tr>
<tr>
<td>$R_{m1}, R_{m3}$</td>
<td>20kΩ, 18kΩ</td>
</tr>
<tr>
<td>$C_{m1}, C_{m2}, C_{m3}, C_{cb}$</td>
<td>1pF, 0.6pF, 0.3pF, 0.2pF</td>
</tr>
</tbody>
</table>

Table 6: Comparison of bias currents of pseudo-class AB and class AB amplifier using adaptive biasing technique.

<table>
<thead>
<tr>
<th></th>
<th>Pseudo-Class AB</th>
<th>Class AB</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_Q @ I_{LOAD} = +12.5mA$</td>
<td>1.22 mA</td>
<td>140μA</td>
</tr>
<tr>
<td>$I_Q @ I_{LOAD} = 0$</td>
<td>119μA</td>
<td>119μA</td>
</tr>
<tr>
<td>$I_Q @ I_{LOAD} = -12.5mA$</td>
<td>44μA</td>
<td>44μA</td>
</tr>
<tr>
<td>CBF @ $I_{LOAD} = +12.5mA$</td>
<td>10.2</td>
<td>89</td>
</tr>
</tbody>
</table>
Table 7: Performance comparison of pseudo-class AB and class AB amplifier with adaptive biasing technique.

<table>
<thead>
<tr>
<th></th>
<th>Pseudo-Class AB</th>
<th>Class AB</th>
</tr>
</thead>
<tbody>
<tr>
<td>Process</td>
<td>.5µ</td>
<td>.5µ</td>
</tr>
<tr>
<td>Load</td>
<td>32Ω</td>
<td></td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>±1.5</td>
<td>±1.5</td>
</tr>
<tr>
<td>Gain</td>
<td>53.7dB</td>
<td>71.9dB</td>
</tr>
<tr>
<td>Unity Gain Frequency</td>
<td>1.16MHz</td>
<td>1.17MHz</td>
</tr>
<tr>
<td>Phase Margin</td>
<td>67°</td>
<td>67°</td>
</tr>
<tr>
<td>Gain Margin</td>
<td>19dB</td>
<td>17.5dB</td>
</tr>
<tr>
<td>Slew Rate+</td>
<td>1.22 V/µs</td>
<td>1.17 V/µs</td>
</tr>
<tr>
<td>Slew Rate−</td>
<td>1.45 V/µs</td>
<td>1.61 V/µs</td>
</tr>
</tbody>
</table>
6 Conclusions

A performance comparison of some of the reported LDOs with the proposed LDO is summarized in Table 8. To our knowledge, this is the first LDO using RNMC.

Table 8: PERFORMANCE COMPARISON OF LDOS

<table>
<thead>
<tr>
<th></th>
<th>[HKB*05]</th>
<th>[ASLP07]</th>
<th>[MMC07]</th>
<th>This Work</th>
</tr>
</thead>
<tbody>
<tr>
<td>Year</td>
<td>2005</td>
<td>2007</td>
<td>2007</td>
<td>2010</td>
</tr>
<tr>
<td>Process (µm)</td>
<td>0.09</td>
<td>0.35</td>
<td>0.18</td>
<td>0.5</td>
</tr>
<tr>
<td>( V_{LINE} ) (V)</td>
<td>1.2</td>
<td>2.0–5.5</td>
<td>1.0–1.8</td>
<td>1.4–4.2</td>
</tr>
<tr>
<td>( V_{OUT} ) (V)</td>
<td>0.9</td>
<td>1.8</td>
<td>0.9</td>
<td>1.21</td>
</tr>
<tr>
<td>( V_{DO} ) (V)</td>
<td>0.3</td>
<td>0.2</td>
<td>0.1</td>
<td>0.2</td>
</tr>
<tr>
<td>( I_{LOAD-MAX} ) (mA)</td>
<td>100</td>
<td>200</td>
<td>50</td>
<td>100</td>
</tr>
<tr>
<td>( \Delta V_{OUT} ) (mV)</td>
<td>90</td>
<td>54</td>
<td>700</td>
<td>120</td>
</tr>
<tr>
<td>( \Delta V_{OUT}/V_{OUT} )</td>
<td>10%</td>
<td>3%</td>
<td>77.8%</td>
<td>9.9%</td>
</tr>
<tr>
<td>( I_Q@I_{LOAD-MAX} ) (µA)</td>
<td>6000</td>
<td>340</td>
<td>1.2</td>
<td>45</td>
</tr>
<tr>
<td>FOM(ps)</td>
<td>32</td>
<td>459</td>
<td>0.036</td>
<td>59</td>
</tr>
<tr>
<td>Current Efficiency</td>
<td>94.3%</td>
<td>99.83%</td>
<td>99.99%</td>
<td>99.95%</td>
</tr>
<tr>
<td>( C_{OUT} ) (V)</td>
<td>600pF</td>
<td>1µF</td>
<td>100pF</td>
<td>100nF</td>
</tr>
<tr>
<td>Regulator Area (mm²)</td>
<td>0.008</td>
<td>0.264</td>
<td>0.090</td>
<td>0.263</td>
</tr>
</tbody>
</table>
We have used a figure of merit (FOM) derived from [HKB+05] as

\[
FOM = \frac{C_{OUT} \Delta V_{OUT} I_{Q@I_{LOAD-MAX}}}{I_{LOAD-MAX}^2},
\]

where lower FOM implies better performance. The proposed LDO has an FOM that is comparable to [HKB+05], inferior to [MMC07], and superior to [ASLP07]. However, [HKB+05] appears to require a regulated input voltage of 1.2V and has a current efficiency of only 94.3%, rendering it unsuitable for battery-powered applications. Next, if we consider percent transient output voltage variation (\(\Delta V_{OUT} / V_{OUT}\%\)), the design in [MMC07] has a value of 78%. Such a large output voltage variation would likely trigger power-on reset circuitry and is hence unsuitable for micro-processors. Increasing \(C_{OUT}\) to reduce \(\Delta V_{OUT}\) in [MMC07] may lead to instability, since the design has no compensation network. In summary, our design is most suitable for mobile battery-powered micro-processor-based applications.

Also a simple but effective scheme for converting a pseudo-class AB amplifier to a true class AB amplifier is introduced in this thesis. The adaptive biasing circuit results in a low-voltage, low-bias current amplifier. Simulation results illustrate the improved operation of the proposed class AB amplifier.

The pseudo-class AB amplifier and the proposed true class AB amplifier shown in Fig. was only simulated. This amplifiers can be easily fabricated and tested in the future. Also the adaptive biasing can be replaced by replica biasing technique in the future in order to reduce cross-over distortion.
REFERENCES


