FULLY INTEGRATED LOW-DROPOUT REGULATORS WITH CLASS-B SLEW-RATE ENHANCEMENT

BY

SRIKAR KRISHNAPURAPU, B.Tech

A report submitted to the Graduate School
in partial fulfillment of the requirements
for the degree
Master of Sciences, Engineering

Specialization in: Electrical Engineering

New Mexico State University
Las Cruces, New Mexico
MARCH 2013
“FULLY INTEGRATED LOW-DROPOUT REGULATORS WITH CLASS-B SLEW-RATE ENHANCEMENT,” a report prepared by SRIKAR KRISHNAPURAPU in partial fulfillment of the requirements for the degree, Master of Sciences has been approved and accepted by the following:

Linda Lacey
Dean of the Graduate School

Chair of the Examining Committee

Date

Committee in charge:

Dr. Paul M. Furth, Associate Professor, Chair.

Dr. Wei Tang, Assistant Professor.

Dr. Jeffrey Beasley, Professor.
ACKNOWLEDGMENTS

I have had a dream of pursuing my higher education with an emphasis on Electrical Engineering since my days in undergraduate studies. In the course of making my dream come true, I landed here at NMSU. I have been fortunate to have Dr. Paul M. Furth as my advisor over this period of two and a half years. I would like to thank him for encouraging me all the time during my Master’s program. He has a very unique skill in teaching stuff to his students, which helped me a lot throughout these years.

I would like to thank Dr. Jeffrey Beasley and Dr. Wei Tang for being part of my committee on such a short notice.

I would also like to thank Dr. Jaime Ramirez-Angulo, Dr. Deva K. Borah, Alex, Mr. Chris Penner, Zetdi Runyan and Dr. Richard Murphy for their support throughout my Master’s program.

I would like to thank my parents Krishnapurapu Lakshmi Nageshwar Rao, Krishnapurapu Sharada Devi and brother Krishnapurapu Srivathsa for their support and encouragement throughout my life. I would like to thank my uncles Sundar Boddupalli, Veera Ganesh and their families for encouraging me in my endeavours. I would also like to thank Bhargavi for supporting and encouraging me. I take this opportunity to thank Rajesh Satyawada for talking me through to stay at NMSU and continue to work with Dr. Furth when I had the feeling that
it was not right. If that did not happen, I would have not successfully completed
my Masters here at NMSU.

My sincere thanks to Sai Prasad Bhimanapalli, Punith Reddy Surkanti,
Venkat Harish Nammi, CHSSR Krishna, Ranjith Kumar Molgu, Sri Harsh Pakala,
Aditya Reddy Madadi, Uma Maheshwar Kasireddy, Vamshidhar Reddy Rajan-
nagari, Srikant Reddy Siddenki, Atique and Mareddy Vaibhav Reddy for their
valuable inputs, help, support and guidance during my Master’s program.

Finally, I thank my friends Lakshmi, Shankar Bhanu, Shankar Vadla, Akil
Karthik, Akil Vadla, Sowmyadeep Kundu, Vamshi Vemuri, Sudheer Reddy Gouni,
Yeshwanth, Aditya Madhira, Harish Valapala, Sundar, Tapaswy, Harvind, Rajesh
Patti and all my other friends for their timely support.

Above all, I am deeply indebted to ‘The Almighty’ for guiding me and
helping me through times of grief and happiness, through out my life.
VITA

March 28, 1989  Born in Hyderabad, India.

Education

2006 - 2010  B.Tech. Electronics and Communications Engineering, JNTU, India

2010 - 2013  MSEE. in Electrical Engineering, New Mexico State University, USA - GPA 3.4/4.0

Experience

Graduate Teaching Assistant, Electrical Engineering, NMSU, Spring 2011, Spring 2012

Graduate Research Assistant, Arrowhead Research Center, NMSU, Spring 2012, Summer 2012, Fall 2012
ABSTRACT

FULLY INTEGRATED LOW-DROPOUT REGULATORS WITH CLASS-B SLEW-RATE ENHANCEMENT

BY

SRIKAR KRISHNAPURAPU, B.Tech

Master of Sciences, Engineering
Specialization in Electrical Engineering
New Mexico State University
Las Cruces, New Mexico, 2013
Dr. Paul M. Furth, Chair

In this work, we introduce a class-B slew-rate enhancement technique to reduce the settling times in very low quiescent current low-dropout (LDO) voltage regulators in a 0.5 μm CMOS process. We first simulated and verified the experimental results from a previous work on LDOs [1]. There were four LDO designs proposed in [1]: a low quiescent current (LIQ) LDO driving an on-chip capacitive load of 100 pF, a second LIQ LDO driving an off-chip load of 4.7 μF, a micro quiescent current (MIQ) LDO driving an on-chip capacitive load of 100 pF and a second MIQ LDO driving an off-chip load of 1 μF. The LIQ LDOs have a quiescent current (IQ) of 5 μA and a maximum load current (IL,MAX) of 50 mA. The MIQ LDOs have a IQ of 0.5 μA and IL,MAX of 5 mA. The output voltage of
the LDOs is 1.5 V. The same specifications are used to redesign the LDOs in our work.

We introduce a class-B slew-rate enhancement (SRE) circuit and eliminate the adaptive current amplifier used in [1]. The SRE comprises of a current comparator and a very wide NMOS transistor. We also employed split-length compensation from the previous work only to the transistors that required such compensation. Line and load transient tests and dropout voltage measurements were done for all four LDO circuits. AC analysis was also done to ensure stability of the circuits.

We have two types of settling times: settling time high \( t_{SH} \) and settling time low \( t_{SL} \). The time taken by the output voltage to settle back to its regulated value with 1% tolerance after an overshoot is defined as settling time high \( t_{SH} \) and the time taken by the output voltage to settle back to its regulated value with 1% tolerance after an undershoot is defined as settling time low \( t_{SL} \). We have reduced the simulated high and low settling times for all the circuits by more than 50% for both line and load transients. We observed that in a few execeptional cases, the settling time was not reduced by a great extent. For example, in the \( LIQ \) LDO with 4.7 \( \mu F \) load capacitance, during load transient the \( t_{SH} \) and \( t_{SL} \) from [1] were 0 \( \mu s \) and 2 \( \mu s \), respectively, whereas for the same circuit in our work, the \( t_{SH} \) and \( t_{SL} \) are 0 \( \mu s \) and 15.2 \( \mu s \) respectively. We have verified the simulated results with hardware measurement with two of the four LDO circuits, in particular, \( LIQ \) LDO with 100 pF load and \( MIQ \) LDO with 1 \( \mu F \) load. An error made during the layout of the other two circuits rendered them impossible to measure, as the pins used to supply bias currents to the two circuits were accidentally shorted to \( V_{SS} \).
# TABLE OF CONTENTS

## LIST OF TABLES

| x |

## LIST OF FIGURES

| xi |

## 1 INTRODUCTION

| 1 |

## 2 LITERATURE REVIEW

| 2.1 Low Drop-Out Voltage Regulator (LDO) | 4 |
| 2.2 Settling Time | 9 |
| 2.3 Source Cross-Coupled Pairs | 10 |
| 2.4 Split-Length Compensation | 12 |
| 2.5 Class-B Push-Pull Output Stage | 13 |
| 2.6 Previous Work from [1] | 15 |
| 2.6.1 Low $I_Q$ LDO with $C_{LOAD} = 4.7 \mu F$ | 15 |
| 2.6.2 Micro $I_Q$ LDO with $C_{LOAD} = 1 \mu F$ | 16 |
| 2.6.3 Low $I_Q$ LDO with $C_{LOAD} = 100 \text{ pF}$ | 18 |
| 2.6.4 Micro $I_Q$ LDO with $C_{LOAD} = 100 \text{ pF}$ | 20 |

## 3 DESIGN AND SIMULATIONS

| 3.1 Common Block Diagram of Our Designs | 22 |
| 3.2 Low Quiescent Current LDO with $C_{LOAD} = 4.7 \mu F$ | 24 |
LIST OF TABLES

2.1 LIQ LDO Transistor Sizing ........................................ 16

3.1 LIQ LDO (4.7 µF) Transistor Sizing .......................... 24
3.2 LIQ LDO (4.7 µF) Component Values ......................... 24
3.3 LIQ LDO (100 pF) Component Values ......................... 32
3.4 LIQ LDO AC Analyses Results ................................. 35
3.5 MIQ LDO (1 µF) Component Values ............................ 36
3.6 MIQ LDO (100 pF) Component Values ......................... 41
3.7 MIQ LDO AC Analyses Results ................................. 44
3.8 Comparison of LIQ LDO Results with [1] ..................... 45
3.9 Comparison of MIQ LDO Results with [1] ..................... 46
4.1 Summary of Experimental Results ............................. 56
5.1 Comparison of Measured Results ............................. 59
# LIST OF FIGURES

<table>
<thead>
<tr>
<th>Figure</th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.1</td>
<td>Block Diagram of a Portable Battery-Powered Mobile Device</td>
<td>1</td>
</tr>
<tr>
<td>2.1</td>
<td>Block Diagram of a Low Drop-Out Voltage Regulator</td>
<td>5</td>
</tr>
<tr>
<td>2.2</td>
<td>LDO Drop-out</td>
<td>6</td>
</tr>
<tr>
<td>2.3</td>
<td>Line Transient</td>
<td>7</td>
</tr>
<tr>
<td>2.4</td>
<td>Load Transient</td>
<td>8</td>
</tr>
<tr>
<td>2.5</td>
<td>Op Amp Settling Time</td>
<td>9</td>
</tr>
<tr>
<td>2.6</td>
<td>Settling Times for Line Transient of an LDO</td>
<td>10</td>
</tr>
<tr>
<td>2.7</td>
<td>Source Cross-Coupled Pair</td>
<td>11</td>
</tr>
<tr>
<td>2.8</td>
<td>NMOS and PMOS Transistors with Split-Length Compensation</td>
<td>13</td>
</tr>
<tr>
<td>2.9</td>
<td>Complimentary Class-B (Push-Pull) Stage</td>
<td>14</td>
</tr>
<tr>
<td>2.10</td>
<td>Low $I_Q$ LDO with 4.7,$\mu$F load</td>
<td>17</td>
</tr>
<tr>
<td>2.11</td>
<td>Adaptive Current Bleeding Circuit</td>
<td>18</td>
</tr>
<tr>
<td>2.12</td>
<td>Micro $I_Q$ LDO with 1,$\mu$F load</td>
<td>19</td>
</tr>
<tr>
<td>2.13</td>
<td>Low $I_Q$ LDO with 100pF load</td>
<td>20</td>
</tr>
<tr>
<td>2.14</td>
<td>Micro $I_Q$ LDO with 100pF load</td>
<td>21</td>
</tr>
<tr>
<td>3.1</td>
<td>Common Block Diagram of Our LDOs</td>
<td>23</td>
</tr>
<tr>
<td>3.2</td>
<td>Class-B Slew-Rate Enhancer Block</td>
<td>23</td>
</tr>
<tr>
<td>3.3</td>
<td>$LI_Q$ LDO with Class-B Output Stage</td>
<td>25</td>
</tr>
</tbody>
</table>
3.4 Dropout Measurement Test Bench LIQ LDO ($C_{LOAD} = 4.7 \mu F$) . 26
3.5 Dropout Measurement for LIQ LDO ($C_{LOAD} = 4.7 \mu F$), $I_L = 50 \text{ mA}$ 27
3.6 Line Transient Test Bench LIQ LDO ($C_{LOAD} = 4.7 \mu F$) . . . . . . 27
3.7 Line Transient Response of LIQ LDO ($C_{LOAD} = 4.7 \mu F$), $I_L = 1 \text{ mA}$ 28
3.8 Ringing in Line Transient Response of LIQ LDO ($C_{LOAD} = 4.7 \mu F$) 28
3.9 Load Transient Test Bench LIQ LDO ($C_{LOAD} = 4.7 \mu F$) . . . . . 29
3.10 Load Transient Response of LIQ LDO ($C_{LOAD}=4.7 \mu F$), $V_{IN} = 2 \text{ V}$ 30
3.11 Ringing in Load Transient Response of LIQ LDO ($C_{LOAD} = 4.7 \mu F$) 30
3.12 AC Analysis Test Bench LIQ LDO ($C_{LOAD} = 4.7 \mu F$) . . . . . 31
3.13 AC Analysis of LIQ LDO ($C_{LOAD} = 4.7 \mu F$), $I_L = 1 \text{ mA}, V_{IN} = 2 \text{ V}$ 31
3.14 Dropout Measurement for LIQ LDO ($C_{LOAD} = 100 \text{ pF}$) . . . . . 32
3.15 Line Transient Response of LIQ LDO ($C_{LOAD} = 100 \text{ pF}$), $I_L = 1 \text{ mA}$ 33
3.16 Ringing in Line Transient Response of LIQ LDO ($C_{LOAD} = 100 \text{ pF}$) 33
3.17 Load Transient Response of LIQ LDO ($C_{LOAD} = 100 \text{ pF}$), $V_{IN} = 2 \text{ V}$ 34
3.18 Ringing in Load Transient Response of LIQ LDO ($C_{LOAD} = 100 \text{ pF}$) 34
3.19 AC Analysis of LIQ LDO ($C_{LOAD} = 100 \text{ pF}$), $I_L = 1 \text{ mA}, V_{IN} = 2 \text{ V}$ 35
3.20 MIQ LDO with Class-B ($C_{LOAD} = 1 \mu F$) . . . . . . . . . . . . . . . . . . 37
3.21 Dropout Measurement for MIQ LDO ($C_{LOAD} = 1 \mu F$) . . . . . 38
3.22 Line Transient Response of MIQ LDO ($C_{LOAD} = 1 \mu F$), $I_L = 1 \text{ mA}$ 38
3.23 Ringing in Line Transient Response of MIQ LDO ($C_{LOAD} = 1 \mu F$) 39
3.24 Load Transient Response of MIQ LDO ($C_{LOAD} = 1 \mu F$), $V_{IN} = 2 \text{ V}$ 39
3.25 Ringing in Load Transient Response of MIQ LDO ($C_{LOAD} = 1 \mu F$) 40
3.26 AC Analysis of MIQ LDO ($C_{LOAD} = 1 \mu F$), $I_L = 1 \text{ mA}, V_{IN} = 2 \text{ V}$ 40
3.27 Dropout Measurement of MIQ LDO ($C_{LOAD} = 100 \text{ pF}$) . . . . . . 41
3.28 Line Transient Response of MIQ LDO ($C_{LOAD} = 100 \text{ pF}$) . . . . . 42

xii
Chapter 1

INTRODUCTION

The driving force behind this work is the increase in usage of portable battery-powered devices. Battery-powered devices require a good power management system, which helps in effective operation. The basic blocks of a power management system, in a portable device, are Battery Charging Circuits, DC-DC Converters, Low-Dropout Regulators and Power Controllers. The basic block diagram of a portable battery-powered mobile device is shown in Fig. 1.1.

![Block Diagram of a Portable Battery-Powered Mobile Device](image)

Figure 1.1: Block Diagram of a Portable Battery-Powered Mobile Device

An LDO is a type of buck converter where the required output voltage is less than the input voltage. One can say that a switching converter, in particular
a buck converter, itself can be used when the output voltage needs to be lower than the input voltage. But considering the cost and complexity of designing a switching converter, LDOs are less expensive and easier to design. LDOs drive many circuits and parts of a mobile device simultaneously. The output of an LDO has to be regulated or maintained the same, even when circuits driven by the LDO are placed in sleep mode. This changes the load current of the LDO. Also, the output of an LDO has to be regulated for any variations in the input voltage, for example, Li - ion battery voltages typically vary from 4.2 V at full charge to 3.0 V at no charge. LDOs are only efficient when $V_{OUT} \geq 0.7V_{IN}$ and switching buck converters are used when the output voltage to input voltage ratio is less than 0.7. All these features make LDOs preferable over switching regulators.

We started our work by reviewing and simulating the four LDO designs proposed in [1] in a 0.5 µm process. We observed that the above designs has one major drawback, namely high settling time. The time taken for the output to go back to its regulated value after it goes higher or lower than the regulated value is known as settling time. For an effective LDO, the settling time should be as low as possible. To reduce settling time for the case that $V_{OUT}$ goes higher than the regulated value, the output node needs to be actively discharged to $V_{SS}$ when the pass element in the LDO turns off.

We have made some changes to the designs proposed in [1] to improve the results. The first two designs are called Low-Quiescent Current LDOs (LIQ-LDOs) and the next two designs are called Micro-Quiescent Current LDOs (MIQ-LDOs). The low-quiescent current designs have 6 μA quiescent current, 400 nA bias current and 50 mA maximum load current each. The difference between the LIQ designs is the load capacitance, the first having 4.7 µF and the second 100 pF. The micro-quiescent current designs have 0.6 μA quiescent current, 40 nA bias
current and 5 mA maximum load current each. Again, the difference between the MIQ designs is the load capacitance, the first having 100 pF and the second 1 µF.

The four circuits proposed in our work have the same values of current and load capacitance as that of the designs in [1].

This report is structured as follows: In Chapter 2, we present a brief introduction to LDOs and source cross-coupled pair. We also analyze the four circuit designs of [1]. In Chapter 3, we explain our LDO designs, their AC models and the simulation results in detail. Chapter 4 deals with experimental measurements and plots. In Chapter 5, we compare our work with other designs and provide conclusion.

In the appendix, we explain the test procedure in detail. We also present Maple work through which we estimate the poles and zeroes of the small signal models of our circuits. We conclude this section with MATLAB codes that were used in plotting simulation and experimental results.
Chapter 2

LITERATURE REVIEW

The research work done here is based on previous work done on Low-Dropout Regulators (LDOs) [1, 2]. The important concepts employed were Split-Length Compensation [3] and Source Cross-Coupled Pairs [4]. As an improvement to the previous work we have added the Class-B operation to the output stage of the LDOs.

In this chapter we discuss Low-Dropout Regulators (LDOs), Settling Time, Split-Length Compensation, Source Cross-Coupled Pairs, Class-B Operation and previous work [1] on which this work is based upon.

2.1 Low Drop-Out Voltage Regulator (LDO)

A linear voltage regulator which supplies a regulated output voltage regardless of any variations in input voltage and output load. An LDO is a low drop-out linear regulator that operates only when the input voltage is slightly greater than the output voltage. Low drop-out indicates that the dropout voltage ranges between 100 mV and 300 mV. Dropout voltage is the difference between the output voltage and input voltage when the output voltage is 100 mV lower than its regulated value.

The basic architecture of an LDO is shown in Fig. 2.1 The basic blocks of an LDO are a voltage reference, error amplifier, pass transistor and feedback network. In our work, the voltage reference is followed by a reference buffer and the error amplifier uses a source cross-coupled input differential pair.
The reference voltage to the LDO can be supplied using an external voltage source or generated on chip using a reference voltage generator. A bandgap reference voltage generator is typically used. The feedback network, which is a voltage divider circuit, comprises of two resistances $R_{F1}$ and $R_{F2}$. It provides a feedback path from the output to the error amplifier. The divided output voltage is compared to the reference voltage.

The error amplifier is one of the most important blocks of an LDO. The error amplifier can be a single-stage or multi-stage differential amplifier, whereas in this work, we use a single-stage amplifier with a source cross-coupled differential pair. The error amplifier generates a voltage based on the difference between its terminals. This voltage is given to the gate of the pass element. The pass element is a very wide PMOS transistor with minimum length. The gate voltage of the pass transistor controls the current through the transistor. This helps in regulating the output voltage. Also, the error amplifier tends to keep its input terminals at the same voltage. So the reference voltage would be the input to the voltage divider.
circuit. Thus, keeping the output voltage constant.

\[ V_{OUT} = V_{REF} \frac{R_{F1} + R_{F2}}{R_{F1}} \]  \hspace{1cm} (2.1)

 Dropout voltage, settling time, overshoot, undershoot, load regulation and line regulation of an LDO are considered to be its most important specifications.

 Dropout voltage has a number of definitions. The definition of dropout voltage used in this work can be explained through the Fig. 2.2

![Figure 2.2: LDO Drop-out](image)

Line regulation is defined as the ratio between the steady-state (SS) change in output voltage to the steady-state (SS) change in input voltage.

\[ \text{Lineregulation} = \frac{\Delta V_{out}}{\Delta V_{in}} \]  \hspace{1cm} (2.2)

Line regulation can be measured by supplying a pulse waveform, with slow rise and fall times, as the input.
As the input voltage transitions from a low value to a high value, the output also tends to go higher than its regulated value for a short period of time. This is known as overshoot. Similarly, as the input voltage goes from a high value down to a low value, the output also tends to go below the regulated value for a short period of time. This is known as undershoot. The time taken by the output voltage to settle back to its regulated value after an overshoot is the settling time high \( t_{SH} \) and the time taken by the output voltage to settle back to its regulated value after an undershoot is the settling time low \( t_{SL} \). Line regulation can be measured from the steady-state change in the regulated output voltage, as shown in Fig. 2.3

\[ \Delta V_{OUT} = \text{Overshoot} + \text{Undershoot} + \Delta V_{OUT,SS} \]

**Figure 2.3: Line Transient**

Load regulation is defined as ratio between the steady-state change in output voltage and the steady-state change in load current.

\[
\text{Loadregulation} = \frac{\Delta V_{out}}{\Delta I_L} \quad (2.3)
\]
Load regulation can be measured by applying a pulsing current waveform at the output.

As the load current transitions from a low value to a high value, the output also tends to go lower than its regulated value for a short period of time. This is known as undershoot. Similarly, as the load current goes from a high value down to a low value, the output also tends to go above its regulated value. This is known as overshoot. The high and low settling time definitions are similar to line regulation, and then settles back as the load current becomes constant. The increase in output voltage is considered as the overshoot and the decrease in output voltage is the undershoot. The time taken by the output voltage to settle back to the regulated value after reaching its minimum value is considered as the settling time. Load regulation can be measured from the steady-state change in the regulated output voltage, as shown in Fig. 2.4

\[ \Delta V_{\text{OUT}, \text{SS}} = \text{Overshoot} + \text{Undershoot} + \Delta V_{\text{OUT}, \text{SS}} \]

Figure 2.4: Load Transient
2.2 Settling Time

Two definitions of settling time are explained in this section. The first definition is of the settling time for an operational amplifier [5] and the second is of the settling time for an LDO [6].

The settling time ($t_s$) for an op amp from [5] is shown in Fig. 2.5. The output voltage of the op amp tends to follow the input voltage. As the input voltage goes high instantly, the output voltage does not change instantly, but gradually follows the input. Here, we have dead time ($t_D$), slew time ($t_{SL}$), recovery time ($t_R$) which also are of importance. Settling time ($t_s$) for an op amp can be defined as the time taken by the output voltage to settle within a tolerance band after a transient in the input. The definition of settling time ($t_s$) is mathematically shown in 2.4.

$$t_s = t_D + t_{SL} + t_R$$  \hspace{1cm} (2.4)

![Figure 2.5: Op Amp Settling Time](image-url)
There are two types of settling time for an LDO: settling time high \((t_{SH})\) and settling time low \((t_{SL})\). The definitions of \(t_{SH}\) and \(t_{SL}\) can be obtained from [6]. The time taken by the output voltage to settle back to within a tolerance band of its regulated value after an overshoot is the settling time high \((t_{SH})\) and the time taken by the output voltage to settle back to within a tolerance band of its regulated value after an undershoot is the settling time low \((t_{SL})\). \(t_{SH}\) and \(t_{SL}\) can be calculated for both line and load transients. Fig. 2.6 shows an example of a line transient of an LDO.

![Figure 2.6: Settling Times for Line Transient of an LDO](image)

2.3 Source Cross-Coupled Pairs

The Source Cross-Coupled Pair (SCCP) is considered efficient in practical circuits as it eliminates any limitations caused by slew-rate. A schematic is shown in Fig. 2.7 from [4]. All the NMOS are sized the same and all the PMOS are sized the same. A current \(I_{BIAS}\) flows through all the transistors in the circuit. Transistors \(M_{11}, M_{21}, M_{31}\) and \(M_{41}\) behave as biasing batteries. \(M_1, M_2, M_3\) and \(M_4\) have the same gate-source voltages as \(M_{11}, M_{21}, M_{31}\) and \(M_{41}\) respectively.
A differential amplifier employing an SCCP can operate in the Class-AB mode with reasonable output currents. The Class-AB operation can be explained as follows: As gate voltage of $M_1$ i.e., $V_{I1}$ increases, the $V_{GS}$ of $M_2$ and $V_{SG}$ of $M_4$ tend to decrease which in-turn reduces the current ($I_{D1}$) through $M_2$ and $M_4$. As $V_{I1}$ increases, the $V_{GS}$ of $M_1$ and $V_{SG}$ of $M_3$ also increase, thus increasing the current ($I_{D2}$) through $M_1$ and $M_3$. Similarly, if $V_{I2}$ is increased, $M_1$ and $M_3$ tend to shut off and $I_{D1}$ increases through $M_2$ and $M_4$. $I_{OUT}$ is given by the following equations:

$$I_{OUT} = I_{D1} - I_{D2}$$  \hspace{1cm} (2.5)$$

$$I_{OUT} = -I_{D2}, \text{as } V_{I1} \text{ increases i.e. } I_{D1} = 0$$  \hspace{1cm} (2.6)$$

Figure 2.7: Source Cross-Coupled Pair
\[ I_{OUT} = I_{D1}, \text{as } V_{I2} \text{ increases i.e. } I_{D2} = 0 \quad (2.7) \]

The slew-rate limitation in \( I_{OUT} \) is as follows:

\[
\text{slewrate} = \frac{dV_{OUT}}{dt} = \frac{-I_{D2}}{C_L}, \text{when } I_{D1} = 0 \quad (2.8)
\]

\[
\text{slewrate} = \frac{dV_{OUT}}{dt} = \frac{I_{D1}}{C_L}, \text{when } I_{D2} = 0 \quad (2.9)
\]

### 2.4 Split-Length Compensation

A number of compensation techniques can be used in a multi-stage amplifier. The complexity of the compensation network increases with the number of stages in the amplifier. Miller compensation, cascode compensation and split-length compensation techniques can be used in cascaded multi-stage amplifiers.

In our work we have used the split-length compensation technique, which is discussed in this section. The reason for choosing split-length compensation over miller and cascode compensation is their drawbacks. Miller compensation introduces a feed-forward path which creates a Right-Half-Plane (RHP) zero. A RHP zero increases the gain by 20dB/decade and drops the phase by 90°. RHP zeros tend to decrease the phase margin thereby degrading the stability of the system. Drawbacks in cascode compensation are: the signal swing is reduced due to two \( V_{DS,SAT} \) drops. A number of bias voltages are used in cascode configurations, increasing the quiescent current in the circuit. Also, in the latest battery powered devices, nano-CMOS processes are preferred for fabricating integrated circuits. In these nano-CMOS processes, supply voltages are very low, making compensation quite a task. Split-length compensation is a good solution for this task.
This technique was introduced by Vishal Saxena and R. Jacob Baker \cite{3}. In this technique, a transistor of length \( L \) is split into two transistors of lengths \( L_1 \) and \( L_2 \) \((L = L_1 + L_2)\). This creates a low impedance node between the two new transistors. Split-length compensation for an NMOS and a PMOS transistor is shown in Fig. 2.8. Considering the NMOS transistors, the bottom transistor \((M_{N,B})\) always operates in triode creating the low-impedance node ”\(X\)”. Similarly in the PMOS transistors, the top transistor \((M_{P,A})\) always operates in triode creating the low-impedance node ”\(Y\)”. 

![Image of NMOS and PMOS Transistors with Split-Length Compensation](image)

Figure 2.8: NMOS and PMOS Transistors with Split-Length Compensation

### 2.5 Class-B Push-Pull Output Stage

The output stages our LDO designs need to be Class-B output stages. This would help in reducing settling time by a huge factor and also increase the efficiency.

Class-B amplifiers improve the efficiency of the circuit by operating the transistors even at very low Q-point currents. A complimentary class-B stage from \cite{7} is shown in Fig. 2.9. The PMOS transistor \(M_1\) operates as a source.
follower for the negative part of the input signal and the NMOS transistor $M_2$ operates as a source follower for the positive part of the input signal.

![Figure 2.9: Complimentary Class-B (Push-Pull) Stage](image)

Consider a pulse waveform is supplied as the input to the stage. For the positive half of the input, $M_2$ turns on and supplies current to the load and for the negative half of the input, $M_1$ turns on and draws current off the output node. This creates the push-pull operation at the output. Since the gate voltages of both the transistors are equal, only one of them can be on at a time.

Each transistor is turned on for half the time, increasing the efficiency of the circuit. However, there is a drawback with a class-B push-pull stage. For $M_1$ to turn on, its $V_{GS}$ must be lower than $V_{TP}$ and for $M_2$ to turn on, its $V_{GS}$ must be greater than $V_{TN}$. So for a condition where $V_{GS}$ is in between, there would be a dead zone in the voltage characteristics of the class-B push-pull stage. This means that neither transistor is conducting for the condition $V_{TP} \leq V_{GS} \leq V_{TN}$. The current through the output stage is always zero.

In the next section, we are going to discuss about the previous work [1] on which our work is based upon and expose the drawbacks in their design.
2.6 Previous Work from [1]

In [1], the author introduces four designs of low power LDOs. The author calls the first two Low-$I_Q$ LDOs and the other two Micro-$I_Q$ LDOs. As their names state, the Low-$I_Q$ LDOs have a quiescent current of $5\mu A$ and the Micro-$I_Q$ LDOs have a quiescent current of $0.5\mu A$. More specifically, the four designs are: (1) Low-$I_Q$ LDO with $C_{LOAD} = 4.7\mu F$, (2) Low-$I_Q$ LDO with $C_{LOAD} = 100\ pF$, (3) Micro-$I_Q$ LDO with $C_{LOAD} = 1\mu F$ and (4) Micro-$I_Q$ LDO with $C_{LOAD} = 100\ pF$.

All four architectures are similar: they have a reference buffer, an error amplifier using a source cross-coupled pair, a voltage divider circuit and a pass element. All of them use the concept of Split-Length Compensation. The difference among the four circuits can be spotted by observing the particular compensation capacitances used to stabilize the circuits.

In [1], the author explores Split-Length Compensation to: (1) reduce $\Delta V_{OUT}$ for line and load transients for on-chip $C_L = 100\ pF$ (2) reduce total quiescent current, and (3) redesign the LDOs to reduce $\Delta V_{OUT}$ to 5% of $V_{OUT}$ by using a large off-chip capacitance.

2.6.1 Low $I_Q$ LDO with $C_{LOAD} = 4.7\mu F$

The schematic of a low quiescent current LDO with $C_{LOAD} = 4.7\mu F$ is shown in Fig. 2.10. The LDO has four parts: a reference buffer, a resistor divider, an error amplifier (single-stage amplifier with a source cross-coupled differential pair) and an adaptive current amplifier. The LDO is supplied with a bias current of 400 nA. The reference buffer drives the low input impedance error amplifier. The reference buffer is a two-stage op-amp. The resistor divider circuit allows scaling of the reference voltage from 1.2 V to 1.5 V or even higher. The resistors have compensation capacitors in parallel with them to improve phase margin. A number of compensation capacitances and resistors were also added to help
improve transient responses. split-length compensation is added to current mirrors (M11-M14, M7-M10) and to the differential pair (M20-M23). The settling time of the circuit during a transient is improved by including an adaptive current amplifier as shown in Fig. 2.11. Different lengths are used for $M_{27}$ and $M_{28}$ to create an intentional offset voltage. This circuit compares $V_{O1}$ (gate voltage of the pass transistor) and $V_{IN}$, when $V_{O1}$ reaches $V_{IN}$, more current is drawn from $V_{OUT}$ to discharge it quickly, thus reducing the settling time. Transistor sizings of LIQ LDO (4.7 $\mu$F) are shown in Table 5.1.

<table>
<thead>
<tr>
<th>Transistors</th>
<th>W/L ($\mu$m/$\mu$m)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$M_{27}$</td>
<td>7.2/9 (x2)</td>
</tr>
<tr>
<td>$M_{1} - M_{6}$, $M_{15}$, $M_{18}$, $M_{19}$, $M_{24}$ - $M_{26}$, $M_{28}$ - $M_{35}$</td>
<td>7.2/0.9 (x2)</td>
</tr>
<tr>
<td>$M_{16}$, $M_{17}$</td>
<td>7.2/0.9 (x6)</td>
</tr>
<tr>
<td>$M_{36}$, $M_{37}$</td>
<td>7.2/0.9 (x20)</td>
</tr>
<tr>
<td>$M_{10}$ - $M_{14}$, $M_{20}$ - $M_{23}$</td>
<td>7.2/0.6 (x2)</td>
</tr>
<tr>
<td>$M_{9}$</td>
<td>7.2/0.6 (x4)</td>
</tr>
<tr>
<td>$M_{8}$</td>
<td>7.2/0.6 (x6)</td>
</tr>
<tr>
<td>$M_{7}$</td>
<td>7.2/0.6 (x12)</td>
</tr>
<tr>
<td>$M_{Pass}$</td>
<td>12000/0.6</td>
</tr>
</tbody>
</table>

### 2.6.2 Micro $I_Q$ LDO with $C_{LOAD} = 1$ $\mu$F

The schematic of a micro quiescent current LDO with $C_{LOAD} = 1$ $\mu$F is similar to that of the LIQ LDO with $C_{LOAD} = 4.7$ $\mu$F, as shown in Fig. 2.12. There are a few differences between the two, which are: split-length compensation is added to transistors $M_3$ - $M_6$, the bias current is reduced to 40 nA and the values of compensation capacitors and resistors are new. Otherwise, the operation of it is similar to the one mentioned above.
Figure 2.10: Low \( I_Q \) LDO with 4.7\( \mu \)F load
Transistor sizings of MIQ LDO (1 $\mu$F) are the same as that shown in Table 5.1 except for $M_{PASS}$ which is sized 1200 $\mu$m/0.6 $\mu$m. In addition, changes are that $M_3 - M_6$ were split into two transistors each "A" and "B". This was done to accommodate split-length compensation in the differential pair. The transistors were split as follows: 7.2 $\mu$m/0.6 $\mu$m with $m=2$ for $M_{3A} - M_{6A}$ in series with $M_{3B} - M_{6B}$ with size 7.2 $\mu$m/0.6 $\mu$m with $m=4$ respectively.

### 2.6.3 Low $I_Q$ LDO with $C_{LOAD} = 100$ pF

The schematic of a low quiescent current LDO with $C_{LOAD} = 100$ pF is similar to that of the $LI_Q$ LDO with $C_{LOAD} = 4.7$ $\mu$F as shown in Fig. 2.13. There are two major differences between the two, namely: the current bleeding circuit is absent in the LDO with lower load and the values of compensation capacitors and resistors are different. The current bleeding circuit is not present here as the load capacitor which the LDO is driving small. The operation is the same as the circuit in $LI_Q$ LDO with $C_{LOAD} = 4.7$ $\mu$F. The sizes of transistors are also the same as LIQ LDO (4.7 $\mu$F).
Figure 2.12: Micro $I_Q$ LDO with 1µF load
2.6.4 Micro $I_Q$ LDO with $C_{LOAD} = 100 \text{ pF}$

The schematic of a micro quiescent current LDO with $C_{LOAD} = 100 \text{ pF}$ is similar to that of the MIQ LDO with $C_{LOAD} = 1 \mu \text{F}$ as shown in Fig. 2.14. The absence of the current bleeding circuit and the values of compensation capacitors and resistors are the differences between MIQ LDO (100 pF) and MIQ LDO (1 $\mu$F). The operation is the same as MIQ LDO with $C_{LOAD} = 1 \mu \text{F}$. The sizes of transistors are also the same as MIQ LDO (1 $\mu$F).
Figure 2.14: Micro $I_Q$ LDO with 100pF load
Chapter 3

DESIGN AND SIMULATIONS

Our work is mainly based on the work done in [1]. Similar to [1], we also have four LDO designs. The load capacitances, bias currents, supply voltages, transistor dimensions for example are the same. The main differences between our four designs and the four designs in [1] are explained in this chapter. We also reveal the subtle changes made in order to obtain improved results. Later in this chapter, we show test benches used to measure load and line transient, dropout voltage, gain margin and phase margin. A comparison of results from our work and the results from [1] is also presented in this chapter.

3.1 Common Block Diagram of Our Designs

All the four LDO designs discussed in this chapter follow a common block diagram which is shown in Fig. 3.1. The first block is the voltage buffer with a voltage divider circuit. This ensures that a fixed reference voltage is fed to the error amplifier. The next block is the error amplifier which is a multi-stage amplifier with a differential source cross-coupled pair. The last stage consists of two blocks: the PMOS pass transistor and the Class-B Slew-Rate Enhancer (Class-B SRE). The PMOS pass transistor is a very wide class-A output stage.

The class-B SRE block consists of two parts: a current comparator and an class-B output stage NMOS transistor as shown in Fig. 3.2. The current source $I_{B1}$ is sourced by the differential inputs of the error amplifier and it is non-linear. The current source $I_{B2}$ is a fixed current source with value $2 \times I_{BIAS}$. In steady state,
the current $I_{B1} = I_{BIAS}$. So the node ”X” is always pulled down as $I_{B2} > I_{B1}$. This keeps $M_N$ turned off. The total current through the current comparator branch at this state is $I_{BIAS}$. During transient the current $I_{B1}$ increases as it is sourced by the differential inputs of the error amplifier leading to the condition: $I_{B1} > I_{B2}$. This pulls the node ”X” high, turning $M_N$ on to pull the output node down. Also the current ($I_N$) through $M_N$ is always zero making it a class-B output stage.

Figure 3.2: Class-B Slew-Rate Enhancer Block
3.2 Low Quiescent Current LDO with $C_{LOAD} = 4.7 \, \mu F$

The schematic of the low quiescent current LDO with a load capacitance of 4.7 $\mu F$ from our work is shown in Fig. 3.3. In our design, we have completely eliminated the adaptive current bleeding circuit seen in Fig. 2.10. Instead, we have added the class-B SRE as shown in Fig. 3.1. The operation of the LDO is similar to the one explained in Section 2.6.1. The sizing of transistors is shown in Table 3.1.

Table 3.1: $LI_Q$ LDO (4.7 $\mu F$) Transistor Sizing

<table>
<thead>
<tr>
<th>Transistors</th>
<th>W/L ($\mu m/\mu m$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$M_1 - M_6, M_{15}, M_{19}, M_{24} - M_{26}$</td>
<td>7.2/0.9 (x2)</td>
</tr>
<tr>
<td>$M_{10} - M_{14}, M_{21}, M_{23}$</td>
<td>7.2/0.6 (x2)</td>
</tr>
<tr>
<td>$M_{9}, M_{20}, M_{22}$</td>
<td>7.2/0.6 (x4)</td>
</tr>
<tr>
<td>$M_{8}, M_{28}$</td>
<td>7.2/0.6 (x6)</td>
</tr>
<tr>
<td>$M_{7}$</td>
<td>7.2/0.6 (x12)</td>
</tr>
<tr>
<td>$M_{27}$</td>
<td>7.2/1.05 (x4)</td>
</tr>
<tr>
<td>$M_{N}$</td>
<td>40/0.75 (x1)</td>
</tr>
</tbody>
</table>

The values of capacitances and resistances are shown in Table 3.2.

Table 3.2: $LI_Q$ LDO (4.7 $\mu F$) Component Values

<table>
<thead>
<tr>
<th>Component</th>
<th>Value</th>
<th>Component</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{C1}$</td>
<td>30 pF</td>
<td>$C_{C6}$</td>
<td>100 fF</td>
</tr>
<tr>
<td>$C_{C2}$</td>
<td>70 pF</td>
<td>$R_{C1}$</td>
<td>850 k$\Omega$</td>
</tr>
<tr>
<td>$C_{C3}$</td>
<td>2 pF</td>
<td>$R_{F1}$</td>
<td>750 k$\Omega$</td>
</tr>
<tr>
<td>$C_{C4}$</td>
<td>3.25 pF</td>
<td>$R_{F2}$</td>
<td>3 M$\Omega$</td>
</tr>
<tr>
<td>$C_{C5}$</td>
<td>8 pF</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Figure 3.3: LIQ LDO with Class-B Output Stage
3.2.1 Dropout Voltage Measurement

The schematic of the test bench for dropout voltage measurement is shown in Fig. 3.4. The two transistors at the output of the LDO form a current mirror used to mirror current to the output. The inductor (10 nH) in series with the resistor (200 mΩ) replicate the impedances of the bonding wires. In order to reduce the total impedance, four branches were attached in parallel. The 600 fF capacitance is the total capacitance of all the pads to the substrate. The 50Ω resistance is the source resistance of the reference voltage, $V_{REF}$.

![Figure 3.4: Dropout Measurement Test Bench LIQ LDO ($C_{LOAD} = 4.7 \mu F$)](image)

A triangular input voltage, with rise and fall times of 50 ms, that goes from 0 V to 2 V is supplied to $V_{IN}$. Bias and load currents were supplied through resistors. $V_{SS1}$ is set to -1 V. The dropout voltage measurement for LIQ LDO ($4.7 \mu F$) is shown in Fig. 3.5. The simulated dropout voltage ($V_{DO}$) measured is 126 mV.

3.2.2 Line Transient Analysis

The schematic of the test bench for Line Transient Analysis is shown in Fig. 3.6. Here, we apply a pulse waveform that varies from 2 V to 2.8 V with rise and fall times of 100 ns at the input. The load current is kept constant at 1 mA.
Figure 3.5: Dropout Measurement for LIQ LDO ($C_{LOAD} = 4.7 \, \mu F$), $I_L = 50 \, mA$

Figure 3.6: Line Transient Test Bench LIQ LDO ($C_{LOAD} = 4.7 \, \mu F$)

We define the settling time high ($t_{SH}$) as the time from when the output voltage reaches its highest value till it settles to within 1% of the regulated value. Similarly, we define the settling time low ($t_{SL}$) as the time from when the output voltage reaches its lowest value till it settles to within 1% of the regulated value. Using the test bench of Fig. 3.6, we measure the total change in the output voltage ($\Delta V_{OUT} = V_{OUT,MAX} - V_{OUT,MIN}$) as well as high and low settling times. Fig. 3.7
shows the line transient response for $LI_Q$ LDO ($4.7 \, \mu F$). Details of the ringing in the output voltage after overshoot and undershoot are shown in Fig. 3.8.

**Figure 3.7:** Line Transient Response of $LI_Q$ LDO ($C_{LOAD} = 4.7 \, \mu F$), $I_L = 1mA$

**Figure 3.8:** Ringing in Line Transient Response of $LI_Q$ LDO ($C_{LOAD} = 4.7 \, \mu F$)

### 3.2.3 Load Transient Analysis

The schematic of the test bench for Load Transient Analysis is shown in Fig. 3.9. Here, we apply a voltage pulse, with rise and fall times of 133 ns through a 104 $\Omega$ resistor. The variation of the voltage pulse is set in such a way that the
current through the resistance varies from 0 to 12.5 mA. The 12.5 mA current is then multiplied four times through the current mirror setup. As such, the load current of the LDO varies from 0 to 50 mA. The input voltage $V_{IN}$ is kept constant at 2 V.

Here we measure the settling time high ($t_{SH}$) and settling time low ($t_{SL}$) and also $\Delta V_{OUT}$. Fig. 3.10 shows the load transient response for $LIQ$ LDO (4.7 $\mu$F). Details of the output voltage waveform after overshoot and undershoot are shown in Fig 3.11

![Figure 3.9: Load Transient Test Bench LIQ LDO (CLOAD = 4.7 $\mu$F)](image)

### 3.2.4 AC Analysis

The schematic of the test bench for AC Analysis is shown in Fig. 3.12. We break the loop in the error amplifier using a huge inductor value of 100 MH and a huge capacitance of 1 F. At DC, the circuit is closed, as the inductor blocks AC signals and allows DC signals. So, the circuit is balanced and bias currents are correct. But from the AC point of view, the circuit is open loop.

We plot the gain using a logarithmic plot where the actual value of gain is converted to ”dB” using the formula, $20 \times \log(gain)$. We measure the Gain in dB, Gain Margin (GM) in dB and Phase Margin (PM) in degrees and Unity Gain
Figure 3.10: Load Transient Response of $L_{IQ}$ LDO ($C_{LOAD}=4.7 \ \mu\text{F}$), $V_{IN}=2\ \text{V}$

Figure 3.11: Ringing in Load Transient Response of $L_{IQ}$ LDO ($C_{LOAD}=4.7 \ \mu\text{F}$)

Frequency (UGF) in kHz. Fig. 3.13 shows the AC analysis for $L_{IQ}$ LDO with $C_{LOAD}=4.7 \ \mu\text{F}$.

3.3 Low Quiescent Current LDO with $C_{LOAD}=100 \ \text{pF}$

The schematic of the low quiescent current LDO with a load capacitance of 100 pF from our work is the same as the one shown in Fig. 3.3. The only
difference is the values of capacitances and resistors. The sizing of transistors, the bias currents etc., are exactly the same as that of Section 3.2.

The values of capacitances and resistances are shown in Table: 3.3

### 3.3.1 Dropout Voltage Measurement

The schematic of the test bench for dropout voltage measurement of LIQ LDO with $C_{LOAD} = 100$ pF is the same as that of Section 3.2.1
Table 3.3: $LI_Q$ LDO (100 pF) Component Values

<table>
<thead>
<tr>
<th>Component</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{C1}$</td>
<td>11 pF</td>
</tr>
<tr>
<td>$C_{C2}$</td>
<td>20 pF</td>
</tr>
<tr>
<td>$C_{C3}$</td>
<td>0</td>
</tr>
<tr>
<td>$C_{C4}$</td>
<td>0</td>
</tr>
<tr>
<td>$C_{C5}$</td>
<td>0</td>
</tr>
<tr>
<td>$C_{C6}$</td>
<td>2 pF</td>
</tr>
<tr>
<td>$R_{C1}$</td>
<td>150 kΩ</td>
</tr>
<tr>
<td>$R_{F1}$</td>
<td>750 kΩ</td>
</tr>
<tr>
<td>$R_{F2}$</td>
<td>3 MΩ</td>
</tr>
</tbody>
</table>

The dropout voltage measurement of $LI_Q$ LDO with $C_{LOAD} = 100$ pF is shown in Fig. 3.14. The dropout voltage ($V_{DO}$) measured is 125.1 mV.

![Figure 3.14: Dropout Measurement for $LI_Q$ LDO ($C_{LOAD} = 100$ pF)](image-url)
3.3.2 Line Transient Analysis

The schematic of the test bench for line transient response of \( LIQ \) LDO with \( C_{LOAD} = 100 \text{ pF} \) is the same as that of Section 3.2.2. The line transient response of \( LIQ \) LDO with \( C_{LOAD} = 100 \text{ pF} \) is shown in Fig. 3.15. Details of the output voltage after overshoot and undershoot are shown in Fig. 3.16.

![Figure 3.15: Line Transient Response of \( LIQ \) LDO (\( C_{LOAD} = 100 \text{ pF} \)), \( I_L = 1 \text{ mA} \)](image)

![Figure 3.16: Ringing in Line Transient Response of \( LIQ \) LDO (\( C_{LOAD} = 100 \text{ pF} \))](image)
3.3.3 Load Transient Analysis

The schematic of the test bench for load transient response of $LIQ$ LDO with $C_{LOAD} = 100$ pF is the same as that of Section 3.2.3.

The load transient response of $LIQ$ LDO with $C_{LOAD} = 100$ pF is shown in Fig. 3.17. Details of the output voltage after overshoot and undershoot are shown in Fig 3.18.

Figure 3.17: Load Transient Response of $LIQ$ LDO ($C_{LOAD} = 100$ pF), $V_{IN} = 2$ V

Figure 3.18: Ringing in Load Transient Response of $LIQ$ LDO ($C_{LOAD} = 100$ pF)
3.3.4 AC Analysis

The schematic of the test bench for load transient response of L\textsubscript{IQ} LDO with $C_{LOAD} = 100$ pF is the same as that of Section 3.2.4. The results of AC analysis of LDO with $C_{LOAD} = 100$ pF are shown in Fig. 3.19.

![AC Analysis Graph](image)

Figure 3.19: AC Analysis of L\textsubscript{IQ} LDO ($C_{LOAD} = 100$ pF), $I_L = 1$ mA, $V_{IN} = 2$ V

The results from AC analyses of the two L\textsubscript{IQ} LDOs are shown in the Table 3.4.

<table>
<thead>
<tr>
<th></th>
<th>L\textsubscript{IQ} LDO (4.7 µF)</th>
<th>L\textsubscript{IQ} LDO (100 pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain (dB)</td>
<td>78.42</td>
<td>78.2</td>
</tr>
<tr>
<td>GM (dB)</td>
<td>105.8</td>
<td>12.5</td>
</tr>
<tr>
<td>UGF (kHz)</td>
<td>18.3</td>
<td>978.6</td>
</tr>
<tr>
<td>PM (Deg.)</td>
<td>50.61</td>
<td>91.48</td>
</tr>
</tbody>
</table>

Note: GM is Gain Margin, UGF is Unity Gain Frequency and PM is Phase Margin.
3.4 Micro Quiescent Current LDO with $C_{LOAD} = 1 \ \mu F$

The schematic of the micro quiescent current LDO with a load capacitance of 1 \ \mu F from our work is shown in Fig. 3.20. In this design for a micro $I_Q$ LDO, we have added split length compensation to transistors $M_4$ and $M_5$ resulting in two extra transistors $M_{30}$ and $M_{29}$. The sizes of the split-length transistors are as follows: 7.2 \ \mu m/0.6 \ \mu m with multiplicity of 2 for $M_4$ and $M_5$ and 7.2 \ \mu m/0.6 \ \mu m with multiplicity of 4 for $M_{30}$ and $M_{29}$.

The bias current supplied is 40 nA and the maximum load current is 5 mA. All other aspects of the circuit are similar to the $LI_Q$ designs except the values of capacitors and resistors used in the design. The values of capacitances and resistances are shown in Table 3.5.

<table>
<thead>
<tr>
<th>Component</th>
<th>Value</th>
<th>Component</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{C1}$</td>
<td>3 pF</td>
<td>$C_{C7}$</td>
<td>500 fF</td>
</tr>
<tr>
<td>$C_{C2}$</td>
<td>60 pF</td>
<td>$C_{C8}$</td>
<td>0</td>
</tr>
<tr>
<td>$C_{C3}$</td>
<td>0</td>
<td>$R_{C1}$</td>
<td>1 MΩ</td>
</tr>
<tr>
<td>$C_{C4}$</td>
<td>3 pF</td>
<td>$R_{F1}$</td>
<td>3 MΩ</td>
</tr>
<tr>
<td>$C_{C5}$</td>
<td>900 fF</td>
<td>$R_{F2}$</td>
<td>12 MΩ</td>
</tr>
<tr>
<td>$C_{C6}$</td>
<td>200 fF</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

All the test benches and testing procedures for $MI_Q$ LDO with $C_{LOAD} = 1 \ \mu F$ are the same as those in Section 3.2. There is one difference that the 1 MΩ resistance at the output is absent.

The dropout voltage measurement of $MI_Q$ LDO with $C_{LOAD} = 1 \ \mu F$ is shown in Fig. 3.21. The dropout voltage ($V_{DO}$) measured is 125 mV.
Figure 3.20: $MI_Q$ LDO with Class-B ($C_{LOAD} = 1 \mu F$)
Figure 3.21: Dropout Measurement for MIQ LDO ($C_{LOAD} = 1 \mu F$)

The line transient response of MIQ LDO with $C_{LOAD} = 1 \mu F$ is shown in Fig. 3.22. Details of the output voltage after overshoot and undershoot in line transient response are shown in Fig. 3.23.

Figure 3.22: Line Transient Response of MIQ LDO ($C_{LOAD} = 1 \mu F$), $I_L = 1 \text{ mA}$
Figure 3.23: Ringing in Line Transient Response of $MI_Q$ LDO ($C_{LOAD} = 1 \mu F$)

The load transient response of $MI_Q$ LDO with $C_{LOAD} = 1 \mu F$ is shown in Fig. 3.24. Details of the output voltage after overshoot and undershoot in load transient response are shown in Fig. 3.25.

Figure 3.24: Load Transient Response of $MI_Q$ LDO ($C_{LOAD} = 1 \mu F$), $V_{IN} = 2 \text{ V}$

Fig. 3.26 shows the results of AC analysis of $MI_Q$ LDO with $C_{LOAD} = 1 \mu F$. 
3.5 Micro Quiescent Current LDO with $C_{LOAD} = 100$ pF

The schematic of the micro quiescent current LDO with a load capacitance of 100 pF the same as that of MIQ LDO with $C_{LOAD} = 1 \mu$F. The only difference is the capacitor and resistor values. Their values are given in Table: 3.6

All the test benches and testing procedures for MIQ LDO with $C_{LOAD} = 100$ pF are the same as those in Section 3.2, with the 1 MΩ resistance absent.
Table 3.6: MIQ LDO (100 pF) Component Values

<table>
<thead>
<tr>
<th>Component</th>
<th>Value</th>
<th>Component</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{C1}$</td>
<td>10 pF</td>
<td>$C_{C7}$</td>
<td>200 fF</td>
</tr>
<tr>
<td>$C_{C2}$</td>
<td>75 pF</td>
<td>$C_{C8}$</td>
<td>162.5 fF</td>
</tr>
<tr>
<td>$C_{C3}$</td>
<td>100 fF</td>
<td>$R_{C1}$</td>
<td>280 kΩ</td>
</tr>
<tr>
<td>$C_{C4}$</td>
<td>0</td>
<td>$R_{F1}$</td>
<td>3 MΩ</td>
</tr>
<tr>
<td>$C_{C5}$</td>
<td>0</td>
<td>$R_{F2}$</td>
<td>12 MΩ</td>
</tr>
<tr>
<td>$C_{C6}$</td>
<td>2 pF</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

The dropout voltage measurement of MIQ LDO with $C_{LOAD} = 100$ pF is shown in Fig. 3.27. The dropout voltage ($V_{DO}$) measured is 125 mV.

![Figure 3.27: Dropout Measurement of MIQ LDO ($C_{LOAD} = 100$ pF)](image)

The line transient response of MIQ LDO with $C_{LOAD} = 100$ pF is shown in Fig. 3.28. Details of the output voltage after overshoot and undershoot in line transient response are shown in Fig. 3.29.
Figure 3.28: Line Transient Response of MI_Q LDO \( (C_{LOAD} = 100 \ pF) \)

Figure 3.29: Ringing in Line Transient Response of MI_Q LDO \( (C_{LOAD} = 100 \ pF) \)

The load transient response of MI_Q LDO with \( C_{LOAD} = 1 \ \mu F \) is shown in Fig. 3.30. Details of the output voltage after overshoot and undershoot in load transient response are shown in Fig. 3.31.

Fig. 3.32 shows the results of AC analysis of MI_Q LDO with \( C_{LOAD} = 100 \ pF \).
Figure 3.30: Load Transient Response of MIQ LDO ($C_{LOAD} = 100$ pF)

Figure 3.31: Ringing in Load Transient Response of MIQ LDO ($C_{LOAD} = 100$ pF)

The results from AC analyses of the two MIQ LDOs are shown in the Table 3.7.
Table 3.7: MIQ LDO AC Analyses Results

<table>
<thead>
<tr>
<th></th>
<th>MIQ LDO (1 µF)</th>
<th>MIQ LDO (100 pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain (dB)</td>
<td>76.6</td>
<td>78.3</td>
</tr>
<tr>
<td>GM (dB)</td>
<td>16.34</td>
<td>11.1</td>
</tr>
<tr>
<td>UGF (kHz)</td>
<td>29.4</td>
<td>50.6</td>
</tr>
<tr>
<td>PM (Deg.)</td>
<td>54.49</td>
<td>91.3</td>
</tr>
</tbody>
</table>

Note: GM is Gain Margin, UGF is Unity Gain Frequency and PM is Phase Margin.

3.6 Comparison of Simulated Results from Our Work with Experimental Results from [1]

A comparison of results for both the LIQ LDOs from our work with the experimental results for the same designs from [1] is shown in Table 3.8.

The comparison of results for both the MIQ LDOs from our work with the experimental results for the same designs from [1] is shown in Table 4.1.
Table 3.8: Comparison of $LI_Q$ LDO Results with $LI_Q$ LDO

<table>
<thead>
<tr>
<th></th>
<th>$LI_Q$ LDO (4.7 µF) [1]</th>
<th>$LI_Q$ LDO (100 pF) [1]</th>
<th>$LI_Q$ LDO (4.7 µF)</th>
<th>$LI_Q$ LDO (100 pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DO}$ (mV)</td>
<td>123</td>
<td>122.5</td>
<td>126</td>
<td>125</td>
</tr>
<tr>
<td>$\Delta V_{OUT}$, Line (mV)</td>
<td>56.69</td>
<td>563.1</td>
<td>55.3</td>
<td>571.2</td>
</tr>
<tr>
<td>$t_{SL}$, Line (µs)</td>
<td>7</td>
<td>6</td>
<td>4.2</td>
<td>3.7</td>
</tr>
<tr>
<td>$t_{SH}$, Line (µs)</td>
<td>27</td>
<td>16</td>
<td>2.4</td>
<td>5.9</td>
</tr>
<tr>
<td>$\Delta V_{OUT}$, Load (mV)</td>
<td>31.8</td>
<td>428</td>
<td>89.8</td>
<td>751</td>
</tr>
<tr>
<td>$t_{SL}$, Load (µs)</td>
<td>2</td>
<td>7.5</td>
<td>15.2</td>
<td>3.3</td>
</tr>
<tr>
<td>$t_{SH}$, Load (µs)</td>
<td>0</td>
<td>93.5</td>
<td>0</td>
<td>4.2</td>
</tr>
<tr>
<td>$I_Q$ (µA)</td>
<td>5</td>
<td>5</td>
<td>5.3</td>
<td>5.28</td>
</tr>
</tbody>
</table>
Table 3.9: Comparison of $MI_Q$ LDO Results with $[1]$

<table>
<thead>
<tr>
<th></th>
<th>$MI_QLDO$ (1 $\mu$F) [1]</th>
<th>$MI_QLDO$ (100 pF) [1]</th>
<th>$MI_QLDO$ (1 $\mu$F)</th>
<th>$MI_QLDO$ (100 pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DO}$ (mV)</td>
<td>122</td>
<td>101</td>
<td>125</td>
<td>125</td>
</tr>
<tr>
<td>$\Delta V_{OUT}$, Line (mV)</td>
<td>48</td>
<td>360.9</td>
<td>42.49</td>
<td>713.9</td>
</tr>
<tr>
<td>$t_{SL}$, Line ($\mu$s)</td>
<td>62</td>
<td>30</td>
<td>8</td>
<td>18.89</td>
</tr>
<tr>
<td>$t_{SH}$, Line ($\mu$s)</td>
<td>4</td>
<td>18</td>
<td>4.1</td>
<td>11.79</td>
</tr>
<tr>
<td>$\Delta V_{OUT}$, Load (mV)</td>
<td>30.69</td>
<td>483.2</td>
<td>51.17</td>
<td>692.6</td>
</tr>
<tr>
<td>$t_{SL}$, Load ($\mu$s)</td>
<td>4</td>
<td>29</td>
<td>7.3</td>
<td>17</td>
</tr>
<tr>
<td>$t_{SH}$, Load ($\mu$s)</td>
<td>0</td>
<td>51</td>
<td>0</td>
<td>4.2</td>
</tr>
<tr>
<td>$I_Q$ ($\mu$A)</td>
<td>0.5</td>
<td>0.5</td>
<td>0.53</td>
<td>0.53</td>
</tr>
</tbody>
</table>
Chapter 4

LAYOUT & EXPERIMENTAL RESULTS

This chapter contains the layouts and micrographs of our four LDO designs. Later it shows the experimental setups and then hardware measurements of the dropout voltage, quiescent current and line and load transients.

4.1 Layout

The four LDOs discussed in Chapter 3 were designed and simulated in the Cadence design environment. They were fabricated through MOSIS in the ON-Semi 0.5 $\mu$m CMOS process.

The layout of the pass transistors used in the $LI_Q$ and $MI_Q$ designs are shown in Figs. 4.1 and 4.2, respectively. Common-centroid technique is used in layout of differential pairs to match the differential pairs and in the layout of current mirrors to precisely mirror the currents. The layout of $LI_Q$ LDO (4.7 $\mu$F) is shown in Fig. 4.3. The total area is 592.5 x 551.1 $\mu$m$^2$. The layout of $LI_Q$ LDO (100 $p$F) is shown in Fig. 4.4. The total area is 349.95 x 499.05 $\mu$m$^2$. The layout of $MI_Q$ LDO (1 $\mu$F) is shown in Fig. 4.5. The total area is 595.05 x 363.3 $\mu$m$^2$. The layout of $MI_Q$ LDO (100 $p$F) is shown in Fig. 4.6. The total area is 595.05 x 394.2 $\mu$m$^2$. The pad frame containing all four LDO designs is shown in Fig. 4.7.

4.2 Test Apparatus

The list of equipment used for testing the LDOs is given in this section.
Figure 4.1: Pass Transistor used in \( LIQ \) LDOs \((\frac{12000}{0.6})\mu m\)

**Function Generator:** Agilent: 33120A: 15 MHz Function/Arbitrary Waveform Generator. The function generator is used for generating the input signals/waveforms to control the load current and supply voltage.

**Oscilloscope:** Hewlett Packard: 54603B: 60MHz, Digital Storage Oscilloscope. The oscilloscope is used for capturing input and output waveforms for line and load transient responses.

**DC Power Supply:** Agilent: E3631A: 0-6 V, 5A/, 025V, 1A Triple Output DC Power Supply. The DC power supply is used to provide the input, load and bias voltages.
Digital Multimeter: Agilent: 34401A: 6½ Digital Multimeter. The digital multimeter is used to measure DC input and output voltages.

4.3 Experimental Setup

All four LDO topologies should be tested with as little parasitic capacitance as possible. Hence, the idea of testing the LDOs on a breadboard was ruled out. Instead, the LDOs were tested using a full-custom PCB (Printed Circuit Board) which has parasitic capacitance much lower than a breadboard. The full-custom PCB was obtained from [2]. The testing procedure for all four LDO topologies is outlined in Appendix A.
Figure 4.3: $LI_Q\ LDO$ with Class-B SRE ($C_{LOAD} = 4.7 \mu F$)

Figure 4.4: $LI_Q\ LDO$ with Class-B SRE ($C_{LOAD} = 100 \ pF$)
Figure 4.5: MI_Q LDO with Class-B SRE ($C_{LOAD} = 1 \mu F$)

Figure 4.6: MI_Q LDO with Class-B SRE ($C_{LOAD} = 100 \ pF$)
4.4 Experimental Results

This section provides dropout, line and load hardware measurements for two of the four LDO designs. The designs $LI_Q$ LDO driving a 4.7 $\mu$F load and $MI_Q$ LDO driving a 100 pF load could not be tested due to an accidental error made during layout. The pins supplying the bias currents to the two circuits were shorted to $V_{SS}$. 
The experimental dropout voltage measurements of $LI_Q$ LDO with a $C_{LOAD}$ of 100 pF and $MI_Q$ LDO with a $C_{LOAD}$ of 1 µF are shown in Figs. 4.8 and 4.9 respectively. The dropout voltages measured for the two circuits are 123 mV and 141 mV, respectively. The results were plotted using the codes given in Appendix B.

Figure 4.8: Dropout Voltage Measurement of $LI_Q$ LDO ($C_{LOAD} = 100$ pF)

Figure 4.9: Dropout Voltage Measurement of $MI_Q$ LDO ($C_{LOAD} = 1$ µF)
The experimental line transient responses of LIQ LDO with a $C_{LOAD}$ of 100 pF and MIQ LDO with a $C_{LOAD}$ of 1 μF are shown in Figs. 4.10 and 4.11 respectively. The results were plotted using the codes given in Appendix B.

The blip at the rising edge of the input is due to the 50 Ω source impedance at $V_{IN}$. The $\Delta V_{OUT}$ (during line transient) measured for the two circuits are 594 mV and 55.6 mV, respectively. The $t_{SH}$ and $t_{SL}$ for LIQ LDO with a $C_{LOAD}$ of 100 pF are measured as 7.15 μs and 3.7 μs, respectively. The $t_{SH}$ and $t_{SL}$ for MIQ LDO with a $C_{LOAD}$ of 1 μF are measured as 1.5 μs and 8.5 μs, respectively.

![Figure 4.10: Line Transient Response of LIQ LDO (C_{LOAD} = 100 pF)](image)

The experimental load transient responses of LIQ LDO with $C_{LOAD} = 100$ pF and MIQ LDO with $C_{LOAD} = 1$ μF are shown in Figs. 4.12 and 4.13 respectively. The results were plotted using the codes given in Appendix B.

The $\Delta V_{OUT}$ (during load transient) measured for the two circuits are 585 mV and 54.6 mV, respectively. The $t_{SH}$ and $t_{SL}$ for LIQ LDO with a $C_{LOAD}$ of 100 pF are measured as 6.8 μs and 3.65 μs, respectively. The $t_{SH}$ and $t_{SL}$ for MIQ LDO with a $C_{LOAD}$ of 1 μF are measured as 0 μs and 10.5 μs, respectively.
Table 4.1 summarizes the experimental results from our work for the \( LIQ \) LDO with \( C_{LOAD} = 100 \) pF and \( MIQ \) LDO with \( C_{LOAD} = 1 \) \( \mu F \).
Figure 4.13: Load Transient Response of MIQ LDO ($C_{LOAD} = 1 \mu F$)

Table 4.1: Summary of Experimental Results

<table>
<thead>
<tr>
<th></th>
<th>$LI_QLDO$ (100 pF)</th>
<th>$MI_QLDO$ (1 $\mu F$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{OUT}$ (V)</td>
<td>1.512</td>
<td>1.516</td>
</tr>
<tr>
<td>$V_{DO}$ (mV)</td>
<td>123</td>
<td>141</td>
</tr>
<tr>
<td>$\Delta V_{OUT}$, Line (mV)</td>
<td>594</td>
<td>55.6</td>
</tr>
<tr>
<td>$t_{SL}$, Line ($\mu s$)</td>
<td>3.7</td>
<td>8.5</td>
</tr>
<tr>
<td>$t_{SH}$, Line ($\mu s$)</td>
<td>7.15</td>
<td>1.5</td>
</tr>
<tr>
<td>$\Delta V_{OUT}$, Load (mV)</td>
<td>585</td>
<td>54.6</td>
</tr>
<tr>
<td>$t_{SL}$, Load ($\mu s$)</td>
<td>3.65</td>
<td>10.5</td>
</tr>
<tr>
<td>$t_{SH}$, Load ($\mu s$)</td>
<td>6.8</td>
<td>0</td>
</tr>
<tr>
<td>$I_Q$ ($\mu A$)</td>
<td>5.34</td>
<td>0.52</td>
</tr>
</tbody>
</table>
DISCUSSION AND CONCLUSION

We propose an architecture for fully integrated low dropout regulators, which helps in improving the settling time of the LDOs. The four designs described in this work have similar architectures, except for the compensation components.

We introduce a slew-rate enhancement technique that employs a current comparator and a very wide NMOS transistor at the output stage of the LDOs. The NMOS transistor at the output stage is biased off and is turned on only during positive-going transients of the output node.

We have verified the simulated results of only two of the four LDO circuits with hardware measurements. An error made during the layout of the other two circuits rendered them impossible to measure, as the pins used to supply bias currents to the two circuits were accidentally shorted to $V_{SS}$.

Our goal of reducing the settling times of the LDOs for both line and load transients was achieved, except for a few cases. The settling times were improved to more than 50% for $LI_Q$ LDO and $MI_Q$ LDO driving a $C_{LOAD}$ of 100 pF in comparison with the settling times of the same circuits from [1]. This is the case for both line and load transients. The settling times of $LI_Q$ LDO driving a $C_{LOAD}$ of 4.7 µF and $MI_Q$ LDO driving a $C_{LOAD}$ of 1 µF, for line transient were improved to about 50% compared to [1]. But the low settling time of these circuits for load transient was observed to be increased compared to [1], while the high settling time remained the same as of [1], viz. 0 µs.
Table 5.1 compares the experimental results from our work for the \( L_IQ \) LDO with a \( C_{LOAD} \) of 100 pF and \( M_IQ \) LDO with a \( C_{LOAD} \) of 1 µF with those of the same circuits from [1].

5.1 Future Work

From the results we observe that the high settling time for load transient responses of LDOs with off-chip loads has increased compared to [1]. Introduction of a new controlling technique to draw more current from the output node quickly, would be a possible future work.
Table 5.1: Comparison of Measured Results

<table>
<thead>
<tr>
<th></th>
<th>$LI_{Q,LDO}$ (100 pF)</th>
<th>$MI_{Q,LDO}$ (1 µF)</th>
<th>$LI_{Q,LDO}$ (100 pF)</th>
<th>$MI_{Q,LDO}$ (1 µF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Year</td>
<td>2011</td>
<td>2011</td>
<td>2013</td>
<td>2013</td>
</tr>
<tr>
<td>Process</td>
<td>0.5 µm</td>
<td>0.5 µm</td>
<td>0.5 µm</td>
<td>0.5 µm</td>
</tr>
<tr>
<td>Input Range (V)</td>
<td>2 - 2.8</td>
<td>2 - 2.8</td>
<td>2 - 2.8</td>
<td>2 - 2.8</td>
</tr>
<tr>
<td>$V_{OUT}$ (V)</td>
<td>1.49</td>
<td>1.48</td>
<td>1.5</td>
<td>1.5</td>
</tr>
<tr>
<td>$I_{LOAD,MAX}$ (mA)</td>
<td>50</td>
<td>5</td>
<td>50</td>
<td>5</td>
</tr>
<tr>
<td>$I_{LOAD,MIN}$ (µA)</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>$V_{DO}$ (mV)</td>
<td>122.5</td>
<td>122</td>
<td>123</td>
<td>141</td>
</tr>
<tr>
<td>$ΔV_{OUT}$, Line (mV)</td>
<td>563</td>
<td>48</td>
<td>594</td>
<td>55.6</td>
</tr>
<tr>
<td>$t_{SL}$, Line (µs)</td>
<td>6</td>
<td>62</td>
<td>3.7</td>
<td>8.5</td>
</tr>
<tr>
<td>$t_{SH}$, Line (µs)</td>
<td>16</td>
<td>4</td>
<td>7.15</td>
<td>1.5</td>
</tr>
<tr>
<td>$ΔV_{OUT}$, Load (mV)</td>
<td>428</td>
<td>51.2</td>
<td>585</td>
<td>54.6</td>
</tr>
<tr>
<td>$t_{SL}$, Load (µs)</td>
<td>7.5</td>
<td>7.3</td>
<td>3.65</td>
<td>10.5</td>
</tr>
<tr>
<td>$t_{SH}$, Load (µs)</td>
<td>93.5</td>
<td>0</td>
<td>6.8</td>
<td>0</td>
</tr>
<tr>
<td>$I_Q$ (µA)</td>
<td>5</td>
<td>0.5</td>
<td>5.34</td>
<td>0.52</td>
</tr>
</tbody>
</table>
APPENDIX A

Test Document
A.1 Circuit 1: Low Iq LDO 4.7uF

A.1.1: Measuring Dropout Voltage

1. Place the chip on a PCB to avoid loading the output pins with a 60pF capacitance by placing it on a breadboard.

2. Setup is shown in Figure A1.

3. Connect Vss1 (Pin 12) to ground.

4. Close jumpers J11 and J12 to connect the BJT current mirror to pins 16, 17, 18 and 19 as shown in Figure A1.

5. We need 12.5mA of current to the input branch of the BJT current mirror. So close the jumper J4 to connect resistor R_{ja}. R_{ja} is connected to DC power supply 4 that supplies a voltage of 2V. Value of R_{ja} is chosen to have a current of 12.5mA flow through it.
\[ R_{1a} = \frac{2 - 0.7}{12.5 \times 10^{-3}} = 104 \Omega \]

6. Close the jumpers J9a and J9b to connect resistors \( R_{4c} \) and \( R_{5c} \) respectively. The purpose of this is to make sure that the right amount of current is flowing through the BJTs. The BJT current mirror is built using an IC with part number CA 3046.

7. The value of \( R_{4c} \) and \( R_{5c} \) is given in the Figure A1. Measure the voltage drops across \( R_{1a}, R_{4c} \) and \( R_{5c} \) and complete the table1.

<table>
<thead>
<tr>
<th></th>
<th>Measured ‘R’</th>
<th>Expected ‘I’</th>
<th>Measured Voltage Drop</th>
<th>Computed ‘I’</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R_{1a} )</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( R_{4c} )</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( R_{5c} )</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

8. Apply \( V_{ref1} \) to pin 22. \( V_{ref1} = 1.2V \). This can be done using DC power supply 1.

9. Close jumper J2 to connect the output pins 16,17,18 and 19 to resistor \( R_{2a} \) as shown in Figure A1. The value fo \( R_{2a} \) is chosen in such a way that the current flowing through it is 1uA.

\[ R_{2a} = \frac{1.5}{1 \times 10^{-6}} = 1.5M\Omega \]

10. Close jumper J13 to connect the resistor \( R_{3a} \) to pin 21. This is because we need a bias current of 400nA. \( R_{3a} \) is connected to DC power supply 2, which supplies a voltage of 2V. So, the value of \( R_{3a} \) is chosen in order to have a 400nA current flowing through it.

\[ R_{3a} = \frac{2 - 0.635}{400 \times 10^{-9}} = 3.6125M\Omega \]

Note: This value is higher, so it can be built using multiple resistors.

11. To measure the current flowing through \( R_{3a} \), add a wire connection from \( V_b \) to CMOS Op-Amp follower as shown in Figure A2. Measure the drop from DC
power supply 2 to output of the follower. Measure the voltage drops across $R_{2a}$ and $R_{3a}$ and complete table 2.

<table>
<thead>
<tr>
<th></th>
<th>Measured 'R'</th>
<th>Expected 'I'</th>
<th>Measured Voltage Drop</th>
<th>Computed 'I'</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{2a}$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$R_{3a}$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

12. Connect 10uF tantalum capacitors to pins 13,14,15,21 and 22 to reduce noise (at inputs).

13. Attach a DMM to pin 20. The value of Vout1 can be measured.

14. Attach DC power supply 3 to pins 13,14,15 and vary the voltage slowly from 0V to 2V by hand. Complete the table 3. Measured the dropout voltage using the following equation.

$$V_{DO} = (V_S - V_{OUT})|_{V_{out}=V_{out,max}-100mV}$$

Verify $I_L=50mA$ at dropout voltage.

<table>
<thead>
<tr>
<th>$V_S$ (V)</th>
<th>$V_{OUT}$ (V)</th>
<th>$I_L$ (A)</th>
<th>$V_S$ (V)</th>
<th>$V_{OUT}$ (V)</th>
<th>$I_L$ (A)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td></td>
<td></td>
<td>1.4</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0.2</td>
<td></td>
<td></td>
<td>1.45</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0.4</td>
<td></td>
<td></td>
<td>1.5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0.6</td>
<td></td>
<td></td>
<td>1.55</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0.8</td>
<td></td>
<td></td>
<td>1.6</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
<td>1.65</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1.2</td>
<td></td>
<td></td>
<td>1.7</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1.25</td>
<td></td>
<td></td>
<td>1.8</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1.3</td>
<td></td>
<td></td>
<td>1.9</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1.35</td>
<td></td>
<td></td>
<td>2.0</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
A.1.2: Measuring Ground Current

1. The setup for measuring ground current is shown in Figure A3.

![Figure A2: Op Amp Configuration to Measure Ground Current.](image1)

![Figure A3: Jumper Configuration for Measuring Ground Current.](image2)

2. Open jumper J4 to disconnect $R_{1a}$. Connect DMM between DC power supply 3 and pins 13, 14, 15 to measure current ($i_2$) through $V_{s1}$ at 0A load current (J4 disconnected). Complete table 4.
3. Current through R3a ($i_2$) is known and current through R2a ($i_3$) is also known. So ground current can be calculated as follows:

$$i_{ground} = i_1 + i_2 - i_3$$

Complete table 5.

<table>
<thead>
<tr>
<th>Expected ‘I’</th>
<th>Measured ‘I’</th>
</tr>
</thead>
<tbody>
<tr>
<td>$i_{ground}$</td>
<td>5.2uA</td>
</tr>
</tbody>
</table>

A.1.3: Line Transient Test Procedure

1. The setup is shown in Figure A4.

Figure A4: Jumper Configuration for Line Transient Test on Circuit 1.
2. Open jumper J10 to disconnect capacitor from 13,14,15. (Note: Purpose of this is that the capacitor does not allow Vs to vary with 100ns rise and fall times).

3. Connect jumper J4 to leave R1a (104\,\Omega) connected. Also leave jumpers J9a, J9b connected.

4. Now input a wave varying from 2V to 2.8V with rise and fall times of 100ns and frequency 2.5kHz.

5. After generating waveform, the function generator is connected to pins 13,14,15 (before DC power supply 3). The DC power supply 3 supplies a voltage of 2V. The function generator pulses from 0V to 0.8V. (2V offset voltage is not possible for function generator. The maximum low – level voltage is 0V for function generator).

6. The BJT current mirror setup remains the same and the load current is 50mA.

7. With help of 10x probes observe V_{s1} and V_{out1} (pin 20) waveforms on oscilloscope and measure overshoot, undershoot, line regulation, t\text{rise} and t\text{fall} using cursors.

8. Store the waveforms on Digital scope and save to floppy in x, y data format.

9. Now attach load capacitor of 4.7uF to pins 16,17,18,19 and measure overshoot, undershoot, line regulation, t\text{rise} and t\text{fall}.

10. Store the waveforms on Digital scope and save to floppy in x, y data format.

**A.1.4: Load Transient Test Procedure**

1. The setup is shown in Figure A5.

2. Disconnect 4.7uF external capacitor from pins 16,17,18,19.

3. Connect jumper J10 to connect the capacitor to pins 13,14,15.

4. Disconnect the function generator from pins 13,14,15 and apply a DC voltage of 2V (Vs1) from DC power supply 3.
Figure A5: Jumper Configuration for Load Transient Test on Circuit 1.

5. Disconnect DC power supply 4 and connect the function generator. The input wave varies from 0V to 2V with rise and fall times of 133ns. This is because we need the current flowing through the resistor R_{1a} to be 0 to 12.5mA so that the load current would vary from 0 to 50mA.

6. Detach the oscilloscope from 13,14,15 and connect it across R_{4c} (to observe the load current varying).

7. With the help of 10x probes observe the waveforms at pin20 (Vout1) and voltage drop across R_{4c} and measure the overshoot, undershoot, load regulation, t_{rise} and t_{fall} using cursors.

8. Store the waveforms on Digital scope and save to floppy in x, y data format.

9. Now connect load capacitors 4.7uF and measure overshoot, undershoot, load regulation, t_{rise} and t_{fall}.

10. Store the waveforms on Digital scope and save to floppy in x, y data format.
A.2 Circuit 2: Low Iq LDO 100pF

1. Repeat all steps as of circuit 1 except step 8 (in measuring dropout voltage). Connect the reference voltage $V_{\text{ref}2} = 1.2V$ to pin 11.

2. Open jumpers J11 and J12 and close the jumpers J16 and J17. This will disconnect the BJT current mirror setup from circuit 1 and connect it to circuit 2.

3. Now open jumper J13 and close the jumper J14 to connect the resistor $R_{3b}$ to the power supply and disconnect $R_{3a}$. $R_{3b} = R_{3a} = 3.6125M\Omega$.

4. Open jumper J15 while performing line transient test procedure.

A.3 Circuit 3: Micro Iq LDO 100pF

1. Repeat all steps as of circuit 1 except step 8 (in measuring dropout voltage). Connect the reference voltage $V_{\text{ref}3} = 1.2V$ to pin 33.

2. Open jumpers J16 and J17 to disconnect the BJT current mirror setup from circuit 2 and close the jumpers J20 and J21 to connect the BJT current mirror to circuit 3.

3. Now open jumper J14 and close the jumper J18. This will disconnect the resistor $R_{3b}$ and connect $R_{3c}$ to the power supply. The value of $R_{3c}$ is calculated in such a way that a bias current of 40nA (required for Micro Iq design) flows through it.

$$R_{3c} = \frac{2 - 0.754}{40 \times 10^{-9}} = 31.15M\Omega$$

Note: This value is higher, so it can be built using multiple resistors.

4. Open jumper J2 to disconnect the resistor $R_{2a}$ from the setup.

5. While performing dropout and load transient tests, open the jumpers J9a, J9b and J4 to disconnect $R_{4c}$, $R_{5c}$ and $R_{4a}$ and close the jumpers J8a, J8b and J6 to connect $R_{4b}$, $R_{5b}$ and $R_{1c}$ to the setup.

6. The values of $R_{4b}$ and $R_{5b}$ are given in the figure and the value of $R_{1c}$ is calculated in such a way that the current flowing through it is 1.25mA.

$$R_{1c} = \frac{2 - 0.7}{1.25 \times 10^{-3}} = 1040\Omega$$
7. Open jumper J19 while performing line transient test procedure.

**A.4 Circuit 4: Micro Iq LDO 1uF**

1. Repeat all steps as done for circuit 3 also leaving $V_{\text{ref}3}$ ($V_{\text{ref}4}) = 1.2V$ connected to pin 33 (common reference voltage pin to both circuit 3 and circuit 4).

2. Open jumpers J20 and J21 to disconnect the BJT current mirror setup from circuit 3 and close jumper J24 to connect the BJT current mirror setup to circuit 4.

3. Open jumper J18 and close jumper J22 to disconnect $R_{3c}$ and connect $R_{3d}$ to the power supply. $R_{3d} = R_{3c} = 31.15M\Omega$.

4. Open jumper J23 while performing the line transient test procedure.
APPENDIX B

Matlab Codes
Program to draw the dropout voltage test results

% Author : Srikar Krishnapurapu
% Program to draw the dropout voltage test results.
clc;
clear all;
close all;

% Test data

% Read input test data
V_1 = csvread('ip1.csv');
V_2 = csvread('ip2.csv');

% Read output test data
V1 = csvread('1.csv');
V2 = csvread('2.csv');

% Scaling of input data
Vi1=(V_1(:,1)+V_2(:,1))/2;
Vi2=(Vi1(:,1)*2); % scaled and offset added
% Defining the time scale for input
Ti= find(Vi2);
Ti=(Ti*100E-6);

% Scaling of output data
Vo1=(V1(:,1)+V2(:,1))/2;
Vo2=(Vo1(:,1)*2)+0;
% Defining the time scale for output
T= find(Vo2);
T=(T*100E-6);

% Plotting the input and output waveforms
plot(T,Vi2, 'blue', 'LineWidth',4);
hold on;
plot(T,Vo2, 'black', 'LineWidth',4);
ylabel('V (V)');
xlabel('t (s)');
grid on;
axis([0 100E-3 0 2.2]);
%title('Dropout Measurement LIQ 4.7uF');
Program to draw the line transient test results

% Author: Srikar Krishnapurapu
% Program to draw the line transient test results
clc;
clear all;
close all;

% Read input test data
V_1 = csvread('lineip1.csv');
V_2 = csvread('lineip2.csv');
V_3 = csvread('lineip3.csv');

% Read output test data
V11 = csvread('11.csv');
V12 = csvread('12.csv');
V13 = csvread('13.csv');
V14 = csvread('14.csv');
V15 = csvread('15.csv');
V16 = csvread('16.csv');
V17 = csvread('17.csv');
V18 = csvread('18.csv');
V19 = csvread('19.csv');
V110 = csvread('110.csv');

%Scaling of input data
Vi1=(V_1(:,1)+V_2(:,1)+V_3(:,1))/3;
Vi2=(Vi1(:,1)*4)+0.05; % scaled and offset added

% Defining the time scale for input
Ti= find(Vi2);
Ti=(Ti*1E-6)-0.09E-3;

% Delta_Vin = (max(Vi2) - min(Vi2))*1000

% Scaling of output data

% Average of all the output files read
Vo1=(V11(:,1)+V12(:,1)+V13(:,1)+V14(:,1)+V15(:,1)+V16(:,1)+V17(:,1)+V18(:,1)+V19(:,1)+V110(:,1))/10;
% Multiply the avg. with the scale from CRO and then add the offset to give
% correct output
Vo2=(Vo1(:,1)*0.4/2)+1.5;

Delta_Vout = (max(Vo2) - min(Vo2))*1000 % Finding Delta Vout

% Defining the time scale for output
T= find(Vo2);
T=T*1E-6;

% Finding the time at which overshoot & undershoot occur
[vmax,i1] = max(Vo2);
t1 = T(i1); % time of overshoot
 vmin,i2] = min(Vo2);
t2 = T(i2) %time of undershoot

Vsh=mean(Vo2(300:400)) %regulated o/p value after overshoot
Vsh1=Vsh*0.99 %lower value of 1% tolerance band
Vsh2=Vsh*1.01 %higher value of 1% tolerance band

%condition to find the time at which the output last crosses the tolerance
%band values after overshoot
for i=500:-1:1
    if(Vo2(i) < Vsh1 || Vo2(i) > Vsh2)
        break;
    end
end

t1s = T(i+1); %settling time high

tsh = (t1s-t1) %settling time high

Vsl=mean(Vo2(900:1000)) %regulated o/p value after undershoot
Vsl1=Vsl*0.99 %lower value of 1% tolerance band
Vsl2=Vsl*1.01 %higher value of 1% tolerance band

%condition to find the time at which the output last crosses the tolerance
%band values after undershoot
for i=1000:-1:500
    if(Vo2(i) < Vsl1 || Vo2(i) > Vsl2)
        break;
    end
end

t2s = T(i+1); %settling time low

tsl = (t2s-t2) %settling time low

%Plotting the input and output waveforms
subplot(2,1,1);
plot(Ti,Vi2,'Black','LineWidth',4);
ylabel('Vin (V)');
grid on;
axis([0 900E-6 1.9 2.9]);
title('Input Pulse');
subplot(2,1,2);
plot(T,Vo2,'Black','LineWidth',4);
ylabel('V (V)');
xlabel('t (s)');
grid on;
axis([0 900E-6 1.45 1.55]);
%title('Line Transient MIQ 1uF');
Program to draw the load transient test results

% Author : Srikar Krishnapurapu
% Program to draw the load transient test results

clc;
clear all;
close all;

% Read input test data
V_1 = csvread('loadip1.csv');
V_2 = csvread('loadip2.csv');

% Read output test data
V1 = csvread('1.csv');
V2 = csvread('2.csv');
V3 = csvread('3.csv');
V4 = csvread('4.csv');
V5 = csvread('5.csv');
V6 = csvread('6.csv');
V7 = csvread('7.csv');
V8 = csvread('8.csv');
V9 = csvread('9.csv');
V10 = csvread('10.csv');

% Scaling of input data
Vi1=(V_1(:,1)+V_2(:,1))/2;
Vi2=(Vi1(:,1)*4)+0.05; % scaled and offset added
IL=Vi1*104;

% Defining the time scale for input
Ti= find(Vi2);
Ti=((Ti*1E-6)*0.33)+0.0695E-3;

% Delta_Vin = (max(Vi2) - min(Vi2))*1000

% Average of all the output files read
Vo1=(V1(:,1)+V2(:,1)+V3(:,1)+V4(:,1)+V5(:,1)+V6(:,1)+V7(:,1)+V8(:,1)+V9(:,1)+V10(:,1))/10;

% Multiply the avg. with the scale from CRO and then add the offset to give
% correct output
Vo2=(Vo1(:,1)*0.08/2)+1.5;

Delta_Vout = (max(Vo2) - min(Vo2))*1000  % Finding Delta Vout

% Defining the time scale for output
T= find(Vo2);
T=T*1E-6;

% Finding the time at which overshoot & undershoot occur
[vmax,i1] = max(Vo2);
t1 = T(i1) %time of overshoot
[vmin,i2] = min(Vo2); t2 = T(i2) %time of undershoot

Vsh = mean(Vo2(800:1000)) %regulated o/p value after overshoot
Vsh1 = Vsh * 0.99 %lower value of 1% tolerance band
Vsh2 = Vsh * 1.01 %higher value of 1% tolerance band

%condition to find the time at which the output last crosses the
%band values after overshoot
for i = 1000:-1:200
    if (Vo2(i) < Vsh1 || Vo2(i) > Vsh2)
        break;
    end
end
t1s = T(i+1); tsh = (t1s - t1) %settling time high

Vsl = mean(Vo2(150:200)) %regulated o/p value after undershoot
Vsl1 = Vsl * 0.99 %lower value of 1% tolerance band
Vsl2 = Vsl * 1.01 %higher value of 1% tolerance band

%condition to find the time at which the output last crosses the
%band values after undershoot
for i = 200:-1:100
    if (Vo2(i) < Vsl1 || Vo2(i) > Vsl2)
        break;
    end
end
t2s = T(i+1); tsl = (t2s - t2) %settling time low

%Plotting the input and output waveforms
subplot(2,1,1);
plot(Ti,IL, 'Black', 'LineWidth', 4);
ylabel('IL (mA)');
grid on;
axis([0.07E-3 400E-6 5 55]);
title('Load Current');

subplot(2,1,2);
plot(T,Vo2, 'Black', 'LineWidth', 4);
ylabel('Vout (V)');
grid on;
axis([0.07E-3 400E-6 1.47 1.52]);
title('Load Transient LiQ 4.7uF');
REFERENCES
REFERENCES


