FULLY INTEGRATED SWITCHED CAPACITOR BUCK CONVERTER
WITH HIGH EFFICIENCY AND LOW OUTPUT RIPPLE

BY
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“FULLY INTEGRATED SWITCHED CAPACITOR BUCK CONVERTER WITH HIGH EFFICIENCY AND LOW OUTPUT RIPPLE,” a thesis prepared by SUDHIR REDDY GOUNI in partial fulfillment of the requirements for the degree, Master of Sciences has been approved and accepted by the following:

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DEDICATION

Dedicated to my father Manikya Reddy, mother Seshamma and my brother and sisters.
ACKNOWLEDGMENTS

I would like to thank my parents and friends for their support to complete my Master’s degree.

I would like to thank Dr. Paul Furth and Dr. Jaime Ramirez for their support and encouragement throughout my study at New Mexico State University. I would also like to thank Dr. Jeffrey Beasley for his valuable time and suggestions.
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ABSTRACT

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An Integrated Power Management System is built on a single chip. The blocks of this system include Switched Capacitor (SC) buck converter, Low Drop-Out voltage regulator (LDO), comparator and voltage reference. A high efficiency and extremely low ripple buck converter is designed using a switched capacitor voltage divider which converts 3.3 V down to 1.5 V, while operating at a switching frequency of 15 MHz and a load current range of 10µA to 1 mA. A Low Dropout Voltage regulator (LDO) is used at the output of the SC converter, to reduce the ripple and its output voltage is 1.2V. The LDO quiescent current is 40nA. A control loop is implemented using a clock comparator, which helps in improving the efficiency and regulate the output voltage of LDO. The reference voltage
and currents for the comparator and the LDO are generated using a Bandgap Reference circuit. Also a clock generator is used to generate different clocks for the switching converter. This system has a maximum efficiency of 63% and an output ripple of 20mV at 1mA load current. Efficiencies above 50% are achieved for load currents in the range of 100µA to 1 mA. Compared to an only LDO design in which the maximum possible theoretical efficiency is ratio of input to output voltage, in this case it is about 36 %, this design has much higher efficiency.
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Chapter 1

INTRODUCTION

Power consumption is of a great importance in all battery powered portable electronic device. The efficiency of analog and digital circuits are generally improved by operating at lower power supply voltages. However, due to compatibility and fabrication issues, different circuit blocks on a complex integrated circuit often operate at different voltage levels. As such we require a chip to be powered with several external supplies. Having several external supplies increases the manufacturing cost for incorporating the chip.

One solution is to have on-chip DC-DC conversion. Low drop-out voltage regulators (LDO), inductor-based DC-DC converters and switched capacitor DC-DC converters are the three main types of DC voltage converters.

Highest efficiencies can be achieved by inductor-based DC-DC conversion. But inductor-based supplies are not suitable for implementation on-chip, as high quality large-value inductors cannot be integrated. Moreover, the use of inductors results in magnetic coupling issues.

LDO’s are another type of DC-DC converter. They have become an important part of battery powered systems due to their ability to regulate the output voltage. By regulate we mean that the output voltage is constant irrespective of changes in input voltage and output load current. LDO’s also occupy low area and can be integrated on chip. LDO’s are generally used to drive analog and mixed signal circuit blocks, circuits which are sensitive to power supply ripple.
The efficiency of an LDO is given by the ratio of the output voltage to the input voltage. Therefore the efficiency of the LDO will be high only if the difference between the input and output voltages is small. In addition, the quiescent current of the LDO must be kept very low.

High efficiency on chip-chip DC-DC conversion, when the difference between the input and output voltages is high, is possible by using switched capacitor circuits. Switched capacitor circuits make use of capacitors and switches, which can be fully integrated, for DC-DC conversion.

The main goal of this thesis is to realize on-chip DC-DC conversion with high efficiency. Therefore we used a switched capacitor design in a buck converter. We selected a buck converter architecture with switched capacitor design in which \( V_{\text{out}} = 0.5V_{\text{in}} \). An integrated power management system is designed in this thesis. The block diagram of the integrated power management system is shown in Fig: 1.1. Switched Capacitor buck converter, low drop out voltage regulator, bandgap reference and comparator are the major blocks present in the system.

![Block Diagram of the Integrated Power Management System](image_url)

Figure 1.1: Block Diagram of the Integrated Power Management System
In order to function as a good voltage regulator, the switched capacitor design needs a control scheme. Pulse frequency modulation (PFM) and pulse width modulation (PWM) are the two regulation schemes that are widely used. We made use of the PFM scheme to regulate the output voltage, so as to achieve the widest possible range of load currents.

1.0.1 Unique Contributions of this Thesis

1) First fully-integrated switched-capacitor DC-to-DC converter of the NMSU VLSI laboratory.
2) First fully-implemented power management system, including:
   i) Bandgap voltage reference.
   ii) Current source.
   iii) Switched-capacitor DC-to-DC buck converter.

Feedback Control Circuit:
iv) Low drop-out voltage regulator.
   v) Non-overlapping clock generator.
   vi) Clocked comparator.

1.0.2 Thesis Organization

This thesis is organized as follows. Chapter 2 introduces the three types of DC-DC conversions available and the maximum achievable efficiency in each type. Chapter 2 also describes the operation of different blocks used in our integrated power management system. Chapter 3 describes the design modifications and simulations of different blocks of the integrated system. Test results and the organization of the layout are shown in Chapter 4. Comparison of results and issues that we faced are discussed in Chapter 5. Also the future work and enhancements that can be done to this thesis are discussed.
A DC-DC converter is a device which accepts a DC voltage and produces a different DC voltage. A buck converter is used to produce a lower DC voltage level than the input. It is also called as a step down converter. These converters use a clock signal, active elements as switches, and reactive passive elements to store and release energy. The switches used must be very fast in order to achieve high efficiency at high switching frequencies. There are three types of buck converters. They are the inductor-based converter, switch capacitor converters and low drop-out voltage regulators. All these converters are discussed in this chapter. Controller design methods, which are used to regulate the output voltage, are also discussed.

2.1 Low Drop-Out Voltage Regulators (LDO)

A Low Drop-out Voltage Regulator (LDO) is a linear voltage regulator which can supply regulated or constant, output voltage. It is also called as buck converter. The basic architecture of an LDO is shown in Fig. 2.1. The important blocks of the LDO are a voltage reference, error amplifier, pass transistor and voltage divider.

The voltage divider can be implemented using a simple resistor divider, Rf1 and Rf2. Output voltage is scaled according to the resistor ratio. The voltage reference is typically generated from a Bandgap reference and is used to provide a stable DC voltage. Another important block is the error amplifier. It can be a one-
stage or a multi-stage differential amplifier. The positive terminal is connected to
the resistor divider, so that it forms a negative feedback loop. Negative feedback
is achieved because the gain of the pass transistor is negative. The negative
terminal of the error amplifier is connected to the reference voltage. The error
amplifier generates a signal which is a scaled difference between the reference
voltage and the feedback voltage. This signal is given to the gate of the pass
transistor, which generates current accordingly. Therefore the output voltage will
be constant irrespective of changes in the input voltage and irrespective of changes
in the load current.

\[ V_{out} = V_{ref} \frac{R_f 1 + R_f 2}{R_f 1} \]  

(2.1)

Another important block of the LDO is the PMOS pass transistor. The
gate of the PMOS transistor is connected to the output of the error amplifier. The
source is connected to the input voltage. The drain is connected to the output
load and the feedback resistor divider network. The important characteristics of
the pass element are low voltage drop across the source-drain terminals and high
current handling capability. Therefore, the PMOS transistor is generally huge in
size.

The important specifications of the LDO are drop-out voltage, stability,
line regulation, load regulation and power supply rejection ratio (PSRR). One
definition of dropout voltage is ” The voltage difference between the input and
output voltages when the output is 100mV below its value when the input is at its
nominal value [2].” It can be found by giving a slowly varying triangular signal
to the input of the LDO.
Stability of the LDO can be found using AC analysis, and measuring the phase and gain margins. In general the phase margin and gain margin must be greater than 45° and 10 dB, respectively. Many possible compensation techniques can be used to stabilize the circuit. Miller compensation is widely used. In this technique a capacitor is added between the first and second stage to split the poles. Also at the output of each stage, a series resistor can be added to the capacitor to cancel the right half plane zero in the circuit.
Line and load regulation are other specifications of the LDO. Line regulation indicates the capability of the circuit to keep the output at a steady value irrespective of changes in the input voltage. Line regulation can be found by giving slow variations in the input voltage and observing the change in output voltage.

\[
Line \ regulation = \frac{\Delta V_{\text{out}}}{\Delta V_{\text{in}}} \quad (2.2)
\]

Load regulation indicates the capability of the circuit to handle steady state changes in load values. To find the load regulation, a switch can be used to change the load current values through a pulse. The input voltage of the LDO is kept constant in this test. Load regulation is defined by

\[
Load \ regulation = \frac{\Delta V_{\text{out}}}{\Delta I_L} \quad (2.3)
\]

The efficiency of an LDO is given by

\[
\eta = \frac{P_{\text{out}}}{P_{\text{in}}} = \frac{V_{\text{out}}I_{\text{out}}}{V_{\text{in}}(I_{\text{out}} + I_q)} \quad (2.4)
\]

Assuming \( I_q \ll I_{\text{out}} \), the efficiency simplifies to:

\[
\eta = \frac{V_{\text{out}}}{V_{\text{in}}} \quad (2.5)
\]

If the input voltage is 1.4 V and output voltage is 1.2 V, then the efficiency of the LDO is reasonably good:

\[
\eta = \frac{1.2}{1.4} = 85\% \quad (2.6)
\]
By observing the (2.6) we can see that the efficiency of the LDO is high only when the difference between the input and output voltages is very small. Also the quiescent current must be very small.

2.2 Inductor-based Buck Converters

The key element of the switching converters is the switching action. Power efficiency is critical. The available passive elements are resistive elements, capacitive elements and magnetic devices. Magnetic devices are needed to produce high efficiency converters. Ideally magnetic devices would consume zero power, as their major role is to store and release energy. Fig. 2.3 shows the implementation of a simple buck converter [3].

![Buck Converter Block Diagram](image)

Figure 2.3: Buck Converter Block Diagram from [3]

A single pole double throw (SPDT) switch is connected between the input and output. Maximum efficiency is achieved if the switch is ideal, meaning it has no voltage drop across it. The output of the SPDT switch contains a large AC component which has a fundamental switching frequency component, plus harmonics. Therefore a low pass filter is placed between the switch and output. The low pass filter is formed by using an inductor and a capacitor, with a time constant $\sqrt{LC}$. 
The SPDT switch can be implemented using semiconductor devices. As shown in Fig. [2.4] a PMOS transistor and a diode are used. The switching frequency $f_s$ generally lies in the range of 1 kHz to 1 MHz. The duty cycle D is the fraction of time the switch is ON.

During the first half of the cycle the PMOS switch is ON and the diode is OFF as it is reverse-biased with a voltage of $-V_{in}$. During the second half of the cycle, the PMOS switch is turned OFF and the diode becomes forward-biased as the inductor current makes a path through the diode. The output voltage is calculated by averaging the inductor voltage over one time period $T$ and equating it to zero. The average voltage across the inductor must be zero in steady-state or else the inductor current would eventually be infinite (or zero).

The output voltage of a buck converter is given by

$$V_{out} = DV_{in} \tag{2.7}$$

As the duty cycle D is always less than one, the equation results in a step down voltage. Some assumptions are made for deriving (2.7). PMOS switch and
the diode are assumed to have no voltage drop and also parasitic capacitances are neglected. One important condition that we need to verify is the switching period must be shorter than the time constant $\sqrt{LC}$. If the diode drop alone is considered, then

$$V_{out} = DV_{in} - (1 - D)V_D$$  \hspace{1cm} (2.8)

The input current and average inductor current are derived as

$$<I_L> = <I_{out}>$$  \hspace{1cm} (2.9)

$$<I_{in}> = DI_L$$  \hspace{1cm} (2.10)

$$<I_{out}> = \frac{I_{in}}{D}$$  \hspace{1cm} (2.11)

The efficiency is given by:
By substituting (2.11) and (2.7) in (2.12) we get \( \eta \) as 100%. But in practical implementations efficiencies of 85% to 95% are achievable for a specific load current because of losses due to switching, parasitic capacitances and also equivalent series resistances of the inductor and capacitor.

A controller can be designed to regulate the output by controlling the duty cycle. The only disadvantage of this converter is that the inductor cannot be placed on chip. But the use of an inductor helps in achieving high efficiency. Conversion ratio is the ratio of output voltage to the input voltage. This high efficiency is maintained even for low conversion ratios.

### 2.3 Switched Capacitor (SC) Buck Converters

Switched capacitor (SC) circuits perform voltage conversion using the charge transfer method. SC circuits perform the charge transfer using capacitors and switches. The most common switched capacitor circuits are a buck converter, voltage doubler and voltage inverter. A voltage divider, or buck converter, shown in Fig. 2.6 [1].

During the first half of the switching cycle, capacitor \( C_1 \) is connected to the input voltage source and during the second half of the cycle \( C_2 \) will be connected to the input source, as shown in Fig. 2.7. If we use capacitors of same value the average output voltage is:

\[
V_{outavg} = \frac{V_{in}}{2}
\]  

(2.13)
By observing Fig 2.8 the output voltage ripple can be derived from

\[ i = C \frac{dv}{dt} \]  \hspace{1cm} (2.14)
Figure 2.8: SC Buck converter output voltage waveform

which can be rearranged as

\[ \Delta V_{out} = \frac{I_{out}T}{2C} \]  

(2.15)

Assuming complete charge transfer through the switches, the efficiency is given as

\[ \eta = \frac{P_{out}}{P_{out} + P_{loss}} \]  

(2.16)

As the output power is the average of the output voltage and output current, using the \(2.13\) output power is

\[ P_{out} = \frac{I_{out}V_{in}}{2} \]  

(2.17)

Assuming complete charge transfer, dynamic power consumption due to switching is given as

\[ P_{loss} = fC\Delta V_{out}^2 \]  

(2.18)
Using (2.17) and (2.18), efficiency is derived as

\[ \eta = \left( 1 + \frac{\Delta V_{out}}{V_{in}} \right)^{-1} \]  

(2.19)

From the equation above we can say that efficiency is inversely proportional to the output voltage ripple. High efficiencies are achieved if the switching frequencies are high, capacitors are large and loads are light. Switched capacitor techniques have both advantages and disadvantages. The main advantage comes from the absence of the inductor and thus, no electromagnetic coupling to other circuits. Other important advantage is the size of the circuit becomes much smaller and can be integrated on chip. However, it is difficult to maintain high efficiencies over a wide conversion ratio range. Typical conversion ratios are 0.5 to 0.33.

2.4 Bandgap References

Voltage references are used to generate a constant voltage. These references are used in LDO’s, A/D and D/A converters, RF circuits, etc. The accuracy of these reference circuits is very important as the accuracy of these circuits depends on the accuracy of the reference. The reference voltage must be constant, independent of process, power supply and temperature variations.

2.4.1 Bandgap Voltage References

The main idea in generating a temperature-independent reference is to add two quantities with opposite temperature coefficients with proper weighting [4].

As shown in Fig. 2.9 a voltage reference is weighted as the sum of proportional to absolute temperature (PTAT) and complementary to absolute temperature (CTAT) quantities.
The diode voltage is a CTAT quantity, as the diode voltage decreases with increases in temperature. The diodes reverse saturation current $I_s$ increases exponentially with temperature. The rate of change is $-1.6 \text{ mV/°C}$.

$$V_D = nV_T\ln\frac{I_D}{I_s} \quad (2.21)$$

The thermal voltage is a PTAT quantity. It is a function of temperature and is given by (2.22). As the thermal voltage is directly proportional to temperature, it increases linearly with temperature. The rate of increase is $0.085 \text{ mV/°C}$.

$$V_T = \frac{kT}{q} \quad (2.22)$$
Fig. 2.10 shows the circuit implementation of a CTAT voltage reference. Current mirrors are used to generate reference currents. Cascoded current mirrors are used for good matching. A current mirror has equal currents on both sides.

A start-up circuit is used to initiate current in the current mirror. Initially the current through the start-up circuit is zero and the voltage at the gate of transistor $M_{SU}$ is 0 V. As transistor $M_{SU}$ turns ON, this increases the gate voltage of $M_{p1}$ and increases the gate voltage of $M_{n1}$. Therefore the current starts increasing in each branch, including the start-up circuit. As the current increases through the resistor $R_s$, and the gate of $M_{SU}$ is pulled high. This generates reference currents in all branches.

First a CTAT voltage reference is formed by connecting a diode on one side of the current mirror and resistor on the other side, as shown in Fig. 2.10. As the output voltage $V_{outa}$, shown in (2.23) is the voltage across the resistor which is equal to the diode voltage. As such, a CTAT voltage reference is generated.

$$V_{outa} = nV_T\ln\frac{I_{ref}}{I_s} = I_{ref}R$$  \hspace{1cm} (2.23)$$

Refering to Fig. 2.10, suppose we place K parallel diodes in series with resistor R. Now the voltage drop across the diode can be written as the sum of the drop across the resistor and the drop across the diodes.

$$V_{outa} = V_{D1} = I_{ref}R + V_{D2,k}$$  \hspace{1cm} (2.24)$$

$$I_{ref} = \frac{nV_T\ln(K)}{R}$$  \hspace{1cm} (2.25)$$
From (2.25) we see that the reference current is directly proportional to absolute temperature. Therefore it is a PTAT current reference.

In the next step we copy this current to a third branch with a resistor. As the PTAT current passes through resistor, we generate a PTAT voltage reference. We include a variable $L$ in the resistor value for weighting purposes. The output voltage can be written as

$$V_{ref} = I_{ref}LR = nL\ln(K)V_T \tag{2.26}$$

After this we place $K$ parallel diodes in the third branch, as shown in Fig. 2.11.
Now the reference voltage is sum of the drops across the resistor and parallel diodes and is given by

\[ V_{\text{ref}} = I_{\text{ref}} LR + V_{D3,k} \]  

(2.27)

\[ V_{\text{ref}} = nL\ln(K)V_T + V_{D3,k} \]  

(2.28)

By differentiating with respect to temperature on both sides we get

\[ \frac{\partial V_{\text{ref}}}{\partial T} = n\ln(K)\frac{\partial V_T}{\partial T} + \frac{\partial V_{D3k}}{\partial T} \]  

(2.29)
Substituting

$$\frac{\partial V_T}{\partial T} = 0.085 \text{mV}/\text{C} \quad (2.30)$$

$$\frac{\partial V_{Dak}}{\partial T} = -1.6 \text{mV}/\text{C} \quad (2.31)$$

we can derive the relation between L and K as

$$L = \frac{1.6}{n \ln(K)(0.085)} \quad (2.32)$$

By choosing the value of K we can compute L. n is chosen as 1. And thus we have a reference voltage as a weighted sum of two quantities with opposite temperature coefficients. Therefore the generated voltage reference will be constant irrespective of changes in temperature and process variations.

A bandgap voltage cannot directly supply current to a load because the reference voltage would change. Therefore a buffer is placed at the output.

### 2.4.2 Bandgap Current Reference

Current references can be generated using a voltage reference as shown in Fig. 2.12.

If we want $I_{ref}$ to be independent of T, then R must be temperature independent. This current can be copied to other branches for generating reference currents with different multiplicities as shown in Fig 2.12.

### 2.5 Comparators

A comparator is a circuit which compares two analog signals and produces a binary output signal. A differential op-amp without feedback can be used as
a simple comparator. Since comparators don’t have feedback, we don’t need any compensation. And, as a result, comparators have wide bandwidth.

2.5.1 Comparators with Hysteresis

A comparator is considered a decision making circuit. The symbol of a comparator is shown in Fig. 2.13.
If $V_+$ is greater than $V_-$ then $V_{out} = VDD$ and if $V_+$ is less than $V_-$ then $V_{out} = 0$

Let $V_+$ be the input signal and $V_-$ be a reference voltage. If the input signal of the comparator has some noise and is close to the reference value, even small changes in the input voltage above or below the reference value causes the output to switch between high and low logic levels. This switching may consume a lot of dynamic power. Therefore, a small amount of hysteresis is added to the comparator. Hysteresis is defined as the change in threshold voltage dependent on whether the input is rising or falling. It can be introduced by adding two threshold levels on either side of the zero crossings.

Hysteresis can be added using different methods. One method is to add a positive feedback resistor as shown in Fig. 2.14. A small fraction of the output is fed to the positive input and this adds an offset, thus increasing the threshold value. The amount of hysteresis added in the comparator circuit shown in Fig. 2.14 is

$$V_{hyst} = V_{dd} \frac{R_1}{R_2}$$ \hspace{1cm} (2.33)

### 2.5.2 Clocked Comparators

Comparators are usually classified into two types: continuous-time and clocked, or discrete-time. Continuous-time comparators compare the signals asynchronously. But clocked comparators make the decision either on the rising edge or the falling edge of clock. Clocked comparators can be used for high speed operation. Since most IC designs have a main clock, clocked comparators are found in
many applications such as analog-to-digital converters. Clocked comparators are mainly used in low power applications [5]. A simple clocked comparator is shown in Fig. 2.15.
The first stage of the clocked comparator is a pre-amplifier. As the comparator needs to compare signals which have a difference in the range of millivolts, the signals are amplified using the pre-amplifier. The pre-amplifier is shown as a single stage differential amplifier with diode-connected loads. The bandwidth of the preamplifier must be as large as possible.

The second stage is the decision making circuit and is called a latch. A simple latch can be formed by cross-coupled NMOS transistors. Two back-to-back inverters are used in the decision circuit of Fig. 2.15. Depending on the outputs of the first stage, one of the outputs of the latch will go high and the other low. The second stage outputs are given to an SR latch, which acts a memory that stores the output value for a whole clock period.

2.6 Non-Overlapping Clock Generation

A non-overlapping clock generating circuit takes a clock signal and produces two-phase non-overlapping clocks [4]. A non-overlapping clock generating circuit is shown in Fig. 2.16. The amount of delay can be set by the delay of the NAND gate and the chain of inverters between the NAND gate and the output. For low frequency clocks, a large number of inverters are used to get the required delay. This increases power consumption. The schematic of a non overlapping clock generator is shown in Fig. 2.16. As the clock goes high $\phi_1$ goes high and $\phi_2$ goes low and when clock goes low, $\phi_1$ goes low and then $\phi_2$ will go high. Rise and fall times can be significant when driving large capacitance loads. Therefore a chain of inverters can be used as a part of the delay circuit after $\phi_1$ and $\phi_2$ are generated.

2.7 Controller Design

High efficiency power electronic circuits need an efficient controller design, as they have to produce constant output irrespective of changes in the input
voltage and load current. A controller also contributes to power loss and ultimately reduces the maximum possible efficiency. The main goal of the controller in a DC-DC converters is to make the output voltage insensitive to changes in input voltage, load current, process variations and temperature. This goal can be achieved by controlling the duty cycle. Pulse width modulation and pulse frequency modulation are two methods that are widely used in controller designs.
2.7.1 Pulse Width Modulation (PWM)

PWM is widely used in inductor-based DC-DC converters used for heavy loads. The switching frequency is held constant, but the duty cycle is varied in this method. A block diagram of a pulse width modulator is shown in Fig. 2.18. The different sub-blocks are sensor gain, difference amplifier, pulse width modulator and gate driver. The PWM method is presented in [3].

![Pulse Width Modulation block diagram](image)

Figure 2.18: Pulse Width Modulation block diagram

The sensor gain block usually consists of a resistor divider circuit built with precisely matched resistors. The output of the sensor gain is a scaled version of the output voltage. A differential amplifier is placed next. It compares the output of the sensor gain to a reference voltage $V_{ref}$ and produces an error signal $V_e$. If the feedback is perfect, the error signal will be zero. To guarantee stability of the feedback loop, a compensation circuit is added. Different compensation techniques, such as lead compensation and lag compensation, are used to improve the phase margin and gain margin of the control loop.

The pulse width modulator is used to create a pulse signal that depends on the error signal. A pulse width modulator normally consists of a ramp generator
and a comparator. A ramp signal has a frequency which is equal to the switching frequency of the converter. The comparator compares the error signal with the ramp signal and produces a pulse that has a width that is proportional to $V_c$. This generated pulse signal is given to the gate of the switches in the converter. If the switches are huge, an inverter chain must be added to drive them.

### 2.7.2 Pulse Frequency Modulation (PFM)

Pulse frequency modulation is more appropriate for switched capacitor DC-to-DC converters at light loads. In this method the pulse width of the switching signal is constant but the frequency is varied. The output voltage of the converter is maintained at a required value by changing the frequency of the pulse signal. This method decreases the number of switching events and helps in reducing power consumption. PFM can be implemented as single pulse PFM, multi-pulse PFM and burst mode PFM. The block diagram of burst mode PFM is shown in Fig. 2.19.

![Block diagram of burst-mode PFM regulator](image)

**Figure 2.19:** Block diagram of burst-mode PFM regulator from [6]

As shown in Fig. 2.20, a gain hopping loop can be added to the control loop. A gain hopping loop contains gain set block, comparator and up-down counter. The gain hopping loop controls the gain based on the load current and
input voltage. The counter integrates the number of pulses from the comparator and sets the gain block to increase or decrease the gain accordingly.

The PFM loop consists of an analog comparator and a voltage threshold levels. If the output voltage is below a minimum reference voltage the switches in the converter are turned ON until a maximum threshold voltage value is achieved and then the switches are turned OFF. By controlling the switching, the output voltage is regulated. Waveforms of a burst-mode PFM are shown in Fig. 2.20.

Figure 2.20: Waveforms of burst-mode PFM
Chapter 3

DESIGN AND SIMULATIONS

Design and simulations of the integrated power management system designed in this thesis, are discussed in this chapter.

3.1 Switched Capacitor (SC) Buck Converter

This section deals with the design and simulations of the SC buck converter. This type of converter was introduced in Section 2.3.

3.1.1 Design of SC Buck Converter

The schematic of the SC buck converter is shown in Fig. 3.1. It consists of two capacitors and four switches. The input voltage of our system is 3.3V. The SC buck converter circuit is designed to convert 3.3V down to 1.5V. The main idea was that the SC buck converter must be totally integrated on a single chip. Table 3.1 shows our system specifications.

Both capacitors, the flying capacitor $C_1$ as well as grounded capacitor $C_2$, were chosen as 100pF, due to a serious constraints on chip area. In the selected 0.5-micron process, the flying capacitor $C_1$ must be implemented using poly1 and poly2 layers. The capacitance per unit area is $0.9 \, fF$. As such, a 100pF capacitor occupies $111,111 \, fF/\mu m^2$. Assuming a square layout, the capacitor would measure 0.33 mm on each side. The grounded capacitor $C_2$, can be implemented with a MOS capacitor, with a capacitance per unit area of $2.4 \, fF/\mu m^2$. Assuming a square layout, the moscap would measure 0.2 mm on each side.
The switch $M_{SW1}$ was chosen to be a PMOS transistor because it is connected to the input voltage (3.3V) and the rest were chosen as NMOS, since they are connected to either the output voltage (1.5V) or ground (0V). The switch sizes and the switching frequency are optimized for maximum efficiency at a minimum output voltage of 1.4 V. We also constrained the output voltage ripple to be less than 100 mV. Using switch sizes as given in Table 3.2, the peak efficiency was 76% at 1 mA load current and 15 MHz switching frequency. The operation of the SC buck converter is explained in Section 2.3.

![Figure 3.1: Schematic of the SC Buck Converter](image)

<table>
<thead>
<tr>
<th>Table 3.1: SC Buck Converter Specifications</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_1, C_2$</td>
</tr>
<tr>
<td>$V_{in}$</td>
</tr>
<tr>
<td>Average $V_{out}$</td>
</tr>
<tr>
<td>Maximum ripple</td>
</tr>
<tr>
<td>Max. load current</td>
</tr>
</tbody>
</table>
### Table 3.2: SC Buck converter transistor sizing

<table>
<thead>
<tr>
<th>Switch</th>
<th>size ($W_{\mu m} \times L_{\mu m}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$M_{sw1}$</td>
<td>120/0.6</td>
</tr>
<tr>
<td>$M_{sw2}$</td>
<td>90/0.6</td>
</tr>
<tr>
<td>$M_{sw3}$</td>
<td>90/0.6</td>
</tr>
<tr>
<td>$M_{sw3}$</td>
<td>90/0.6</td>
</tr>
</tbody>
</table>

#### 3.1.2 Simulations of SC buck converter

The input voltage of our system is 3.3V. The system clock has a frequency of 15 MHz with rise and fall times of 5 ns each. Fig. 3.2 shows simulated waveforms of the SC buck converter at a load current of 1 mA. The output voltage ripple is 92 mV.

![SCVD output at 1mA load current](image)

Figure 3.2: Output voltage waveform of SC Buck converter at 1mA load current
A parametric analysis is done to find the efficiency, average output voltage and output voltage ripple as a function of load current. As we can see from Fig. 3.3, the peak efficiency is at a load current of 1 mA. Efficiencies above 50% are achievable for a load currents ranging from of 100\(\mu\)A to 4 mA. Losses due to the non-overlapping clock generator circuit are included in the simulation results.

### 3.1.3 Analysis

The steady-state output voltage and current waveforms are shown in Fig. 3.6 at a load current of 1mA. When the capacitor \(C_1\) is connected to the input, a large amount of charge flows onto the capacitor. The amount of charge depends on the initial voltage across \(C_1\) and the final voltage across \(C_1\). The peak amplitude of the input current is limited to \(2.5J_{out}\) by the switching frequency and the switch resistance. The input current decays exponentially with time constant that depends on the switch resistance, and capacitor \(C_1\) as \(C_1\) is charged. From Fig. 3.6.
we can see that the simulated peak value is about $2.8I_{out}$, slightly higher than the theoretical maximum of $2.5I_{out}$.

The current through capacitor $C_1$ is equal to the input current when it is connected to the input and when it is disconnected from the input, we observe a step change of $2I_{out}$. And then $I_{C1}$ starts decreasing in the other direction. The average current through capacitor $C_2$ is zero, as it charges and discharges over each half cycle.

The root mean square (RMS) value of a pulsing current waveform can be calculated using the formula

$$I_{rms} = \sqrt{\frac{I_{ON}^2 + I_{OFF}^2}{2}}$$  \hspace{1cm} (3.1)

The RMS values for the input currents and currents through the capacitors are calculated using (3.1).
Figure 3.5: Output voltage ripple Vs Load current plot for SC Buck converter

\[ I_{1\text{rms}} = 0.816I_{\text{out}} \]  
(3.2)

\[ I_{C1\text{rms}} = 1.15I_{\text{out}} \]  
(3.3)

\[ I_{C2\text{rms}} = 0.575I_{\text{out}} \]  
(3.4)

The output voltage ripple is due to the AC current through the capacitor. It is calculated by using the formula

\[ i = C \frac{dv}{dt} \]  
(3.5)
Figure 3.6: Simulated waveforms of SC Buck Converter

Observing the current waveform of capacitor $C_2$, the (3.5) can be used to derive the formula

$$\Delta V_{out} = \frac{1}{C_2} \frac{T I_{out}}{4} = \frac{I_{out}}{8fC_2}$$

(3.6)
Substituting the capacitor value of 100pF, frequency of 15MHz and a load current of 1mA, we get a theoretical value of 83mV of output ripple, which is very close to our simulation results.

3.2 Non-Overlapping Clock Generator

This section deals with the design and simulations of the non-overlapping clock generator discussed in Section 2.6.

3.2.1 Design of Non-overlapping Clock Generator

A non-overlapping clock generator is used to generate the three clocks required by the switched capacitor buck converter. The schematic of the clock generator is shown in Fig. 3.7. The inverters after the NAND gate are added to generate sufficient dead time between clocks $S_1$ and $S_2$. To have a dead time of roughly 1 ns, we need to add many inverters between the NAND gate and the output, which increases power consumption. Instead resistors are added in series with the inverters to increase the delay of each stage. As the resistor increases the time constant, the required delay was achieved with only four inverters. Of course we need to add resistors of the same value in the two branches in order for the delay to be symmetric. Also buffers are placed at the output for driving the switches in the converter. As we have one PMOS transistor in the switched capacitor voltage divider, we need an inverted clock $S_1b$ for the first half of the cycle. This clock is generated by taking an extra output, as shown in Fig. 3.7.

PMOS and NMOS transistors are sized the same in the inverters to reduce power consumption. All transistor dimensions of the non-overlapping clock generation circuit are given in Table 3.3.

3.2.2 Simulations of Non-overlapping Clock Generator

A clock signal of frequency 15 MHz with rise and fall times of 5 ns is given as the input. The three output clocks that are generated by the circuit are shown
Figure 3.7: Non-overlapping clock generator

![Non-overlapping clock generator diagram](image)

Table 3.3: Non-overlapping clock generator transistor sizing

<table>
<thead>
<tr>
<th>Component</th>
<th>PMOS (µm x µm)</th>
<th>NMOS (µm x µm)</th>
<th>Multiplicity</th>
</tr>
</thead>
<tbody>
<tr>
<td>Invx 1</td>
<td>1.5/0.6</td>
<td>1.5/0.6</td>
<td>1</td>
</tr>
<tr>
<td>Invx 4</td>
<td>1.5/0.6</td>
<td>1.5/0.6</td>
<td>4</td>
</tr>
<tr>
<td>Invx 8</td>
<td>1.5/0.6</td>
<td>1.5/0.6</td>
<td>8</td>
</tr>
<tr>
<td>NAND 2x1</td>
<td>1.5/0.6</td>
<td>1.5/0.6</td>
<td>1</td>
</tr>
<tr>
<td>R</td>
<td>30 kΩ</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

in Fig. 3.8 Fig. 3.9 shows the primary clocks $S_1$ and $S_2$ with a dead time of about 1 ns between them.

3.3 Long Channel Bandgap Reference

The design procedure for generating a bandgap reference voltage, outlined in Section 2.4, is followed. In this section we explain the procedure for generating bias currents based on the bandgap reference.

3.3.1 Design of Bandgap reference

Diodes are not among the models in the particular 0.5 micron process we used. Therefore, we make use of the $p^+$ (source) to $n^−$ (well) junction of a PMOS transistor for simulating the diode.
The schematic of the long channel bandgap reference is shown in Fig 3.10. The length of the MOS devices is chosen as $3L_{min}$. The current mirror formed by transistors $M_{p1}$ and $M_{p2}$ has a current of 60 nA on both sides. The transistors $M_{p4}$ and $M_{p4c}$ are sized 2x for a current of 120 nA. Transistors $M_{p5}$ and $M_{p6}$ are sized to have two thirds the current of the first branch, that is 40 nA. The sizing of all the MOS transistors is given in Table 3.4.

The bias resistors are calculated for a drop of

$$R_B = \frac{V_{DSsat}}{I_{ref}}$$

(3.7)

where $V_{DS, sat} = 0.2V$ and $I_{ref} = 60nA$. 

![Figure 3.8: Non-overlapping clock generator waveforms](image)
Figure 3.9: Deadtime time between the Clocks

Figure 3.10: Long Channel Bandgap Reference
Table 3.4: Long Channel Bandgap Reference transistor sizing

<table>
<thead>
<tr>
<th>Transistor</th>
<th>size($W\mu m \times L\mu m$)</th>
<th>Multiplicity</th>
</tr>
</thead>
<tbody>
<tr>
<td>$M_{p1}, M_{p1c}$</td>
<td>3/1.8</td>
<td>2</td>
</tr>
<tr>
<td>$M_{p2}, M_{p2c}, M_{p3}, M_{p3c}$</td>
<td>3/1.8</td>
<td>6</td>
</tr>
<tr>
<td>$M_{p4}, M_{p4c}$</td>
<td>3/1.8</td>
<td>12</td>
</tr>
<tr>
<td>$M_{p5}, M_{p5c}, M_{p6}, M_{p6c}$</td>
<td>3/1.8</td>
<td>4</td>
</tr>
<tr>
<td>$M_{n1}, M_{n1c}, M_{n2}, M_{n2c}$</td>
<td>4/1.8</td>
<td>2</td>
</tr>
<tr>
<td>$M_{p2}, M_{p2c}, M_{p3}, M_{p3c}$</td>
<td>3/1.8</td>
<td>6</td>
</tr>
<tr>
<td>$M_{SU}$</td>
<td>1.5/0.6</td>
<td>1</td>
</tr>
<tr>
<td>$M_{N3}$</td>
<td>10/0.6</td>
<td>6</td>
</tr>
</tbody>
</table>

A start-up circuit is required to initiate the current in the current mirror branch. The current through the start-up circuit must be very low so as to consume very low power. Therefore, we would require a huge resistor in the start-up circuit. To save the area we placed an NMOS transistor with its gate connected to the source through a resistance as shown in Fig. 3.10. The switch $M_{SU}$ is a minimum-sized transistor. Sub-threshold leakage current through transistor $M_{su}$ is what feeds the start-up circuit.

Initially we chose $K=8$ and $n=1$. We have twice the current in the third branch, therefore $I_{ref}$ in the third branch is given as

$$I_{ref} = \frac{2nln(\frac{K}{2})V_T}{R}$$  \hspace{1cm} (3.8)
Using the equation above, the output reference is given as

\[ V_{ref} = 2nL \ln \left( \frac{K}{2} \right) V_T + V_{D,s,K} \]  

(3.9)

And by differentiating with respect to temperature on both sides, we have

\[ L = \frac{1.6}{2n ln \left( \frac{K}{2} \right) 0.085} \]  

(3.10)

By substituing K as 8, we get L as 6.8. Therefore we sized R as given in Table. 3.5.

And the output reference voltage will be the weighted sum of PTAT and CTAT quantities and is given by (3.8).

### 3.3.2 Generating Bias Currents

The LDO and buffer used in our integrated system each need a bias current. As current is relatively constant in the current mirror of our bandgap reference circuit shown in Fig. 3.10, this current is copied into other branches for generating these bias currents. The LDO needs a bias current of 40nA. As the current mirror branch has a current of 60 nA, transistors \( M_{p5} \) and \( M_{p6} \) are sized two thirds for a current of 40 nA.

<table>
<thead>
<tr>
<th>Resistor</th>
<th>Value(Ohms)</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R )</td>
<td>1M</td>
</tr>
<tr>
<td>( L \times R )</td>
<td>7M</td>
</tr>
<tr>
<td>( R_B )</td>
<td>4M</td>
</tr>
<tr>
<td>( R_n )</td>
<td>500K</td>
</tr>
</tbody>
</table>

Table 3.5: Long Channel Bandgap Reference Resistor Values
3.3.3 Bandgap Reference Simulations

The input voltage is 3.3 V, the same as the system input voltage. The bias current generated for the LDO in our integrated system is also plotted.

The generated bandgap reference voltage is varied with input voltage and temperature. Fig: 3.11 and 3.12 shows that it is constant, irrespective of the changes in input voltage and temperature. The reference current generated for the LDO is also plotted. The reference current varies by approximately 10% over an input voltage range of 3.0 to 3.6 V, and by 30% over the indicated temperature range.

![Image of graph showing variations with input voltage]

Figure 3.11: Variations with input voltage
3.4 Clocked Comparator

The clocked comparator which is discussed in the section 2.5.2 is used. This section explains the sizing of the transistors and simulations of the clocked comparator.

3.4.1 Design of Clocked Comparator

The schematic of the clocked comparator is shown in Fig. 3.13. Transistors $M_1$ and $M_2$ are sized large for good matching, low noise, and to better amplify the input signals. Transistor $M_5$ – $M_8$ are also sized large because they have the same current as the differential pair. The other transistors are sized minimum, as they act like switches. PMOS and NMOS transistors are minimum sized in the
SR latch to reduce power consumption. The sizes of the transistors are given in Table 3.6.

![Schematic of Clocked Comparator](image)

Figure 3.13: Schematic of Clocked Comparator

<table>
<thead>
<tr>
<th>Transistor</th>
<th>size((W\mu m \times L\mu m))</th>
<th>Multiplicity</th>
</tr>
</thead>
<tbody>
<tr>
<td>(M_1, M_2, M_7, M_8)</td>
<td>6/1.05</td>
<td>2</td>
</tr>
<tr>
<td>(M_5, M_6)</td>
<td>3/1.05</td>
<td>2</td>
</tr>
<tr>
<td>(M_3, M_4, M_9, M_{10})</td>
<td>1.5/0.6</td>
<td>1</td>
</tr>
<tr>
<td>(M_{11}, M_{12}, M_{13}, M_{14}, M_{15}, M_{16}, M_{17}, M_{18})</td>
<td>1.5/0.6</td>
<td>1</td>
</tr>
</tbody>
</table>

Table 3.6: Clocked Comparator transistor sizing
3.4.2 Simulations of clocked comparator

The testbench schematic of the clocked comparator is shown in Fig. 3.14. The input clock of the comparator is the same as the system clock. A reference voltage of 1.2V is given to the negative terminal of the comparator. The positive terminal of the comparator is connected to a pulse of frequency 7.5MHz. The voltage of the pulse input is $1.22 \pm 50 \text{ mV}$ From Fig. 3.15 we can see that on the rising edge of the input clock, the output of the comparator is goes high or low, depending on whether the input pulse is above or below the reference voltage.

3.5 Low Drop-out Voltage Regulator

The LDO used in our integrated was designed in [7]. The schematic of the LDO is shown in Fig. 3.16. It has a low quiescent current of 40 nA and can operate at a maximum load current of 5 mA. Some compensation capacitor values were changed from the original design to improve the gain and phase margins.

The SC buck converter has an average output voltage of 1.5V over a wide load current range. Therefore, AC analysis was done for the LDO with an input voltage of 1.5V, for a load current range of $10\mu A$ to 1 mA. Fig 3.17 shows the phase and gain margins for a range of load currents.
Figure 3.15: Waveforms of Clocked Comparator

Figure 3.16: Schematic of the LDO
3.6 Control Loop

A burst-mode pulse frequency modulation (PFM) control loop is designed to regulate the output voltage of the converter. This section deals with the implementation and simulations of the burst-mode PFM control loop.

3.6.1 Design of Burst-mode PFM control loop

The schematic of the PFM control loop is shown in Fig. 3.18. It consists of a clocked comparator, resistor divider circuit, and an AND gate. The output voltage of the converter is sampled using the resistor divider circuit and given to the comparator. The inverted output voltage of the comparator is given to the AND gate. The system clock is given to other input terminal of the AND gate. The output of the AND gate is connected to the clock input of the clock generator circuit, which generates the clocks required by the SC buck converter.
The resistors are sized huge, so that the current in that branch is minimal. The resistor ratio is determined such that our system clocks are always on at 1mA load current. For a converter output voltage of 1.5V, we will obtain a voltage of 1.35 at \( V_x \) and 1.2V at \( V_y \). At this point, the comparator output \( V_{cn} \) is still high and the clock generator will be ON. If the converter output voltage goes above 1.5 V, then \( V_y \) goes above 1.2 V and the comparator output voltage \( V_{cn} \) goes low and the clock generator will be turned OFF. Therefore our controller helps in regulating the converter output voltage and also decreases the number of switching events at low load currents.

Hysteresis is added to the clocked comparator in the control loop by using two minimum sized switches. The two outputs of the comparator are fed back to the gates of these switches creating positive feedback.

Figure 3.18: Schematic of SC Buck Converter with Burst-mode PFM Control Loop
3.6.2 Simulations of SC Buck Converter with Control loop

The controller along with the SC buck converter are simulated together. All the blocks of the controller are connected to the same input voltage $V_{in}$. The system clock is connected to the AND gate input and also the comparator. Fig. 3.19 shows simulated waveforms of our system at $100\mu A$ of load current.

Figure 3.19: SC Buck converter Waveforms at $100\mu A$ load current

From Fig. 3.19 we can see that the clocks are turned ON if the converter output voltage is below 1.5V and they are turned OFF if the output voltage is above 1.6V. From Fig. 3.20 we can see a difference in the clock pattern for a $500\mu A$ load current. In this case the output voltage stays between 1.4V and 1.5V.
3.7 Integrated System

The various blocks which are designed in this chapter are combined to form a voltage regulator, which has an input voltage of 3.3V and generates an output voltage of 1.2V.

3.7.1 Design and Simulations of the Integrated System

The schematic of the integrated system is shown in Fig. 3.21. It includes the SC buck converter, PFM controller, LDO and bangap reference. The output of the SC buck converter is connected to input of the LDO to reduce the ripple and also regulate the converter output voltage. The bandgap reference circuit provides reference voltages to the comparator and the LDO. The output of the bandgap reference is buffered to reduce noise, which might be coupled to the comparator.
input. The bandgap reference also generates bias currents for the LDO and the buffer.

The integrated system takes an input DC voltage of 3.3V and converts it to an output voltage of 1.2V, at a switching frequency of 15 MHz. Fig 3.22 shows the waveforms of the SC buck converter output voltage and the final LDO output voltage, at a load current of 1 mA. The output voltage ripple is less than 20mV. The SC buck converter converts the input voltage of 3.3V to 1.5V and then the LDO converts the 1.5V converter output voltage to 1.2V. The control loop helps in regulating the output voltage.

Figure 3.21: Schematic of the Integrated System at 1 mA Load current

Fig. 3.22 shows the waveforms of the final output and SC buck converter output in the integrated system. The average of the final output voltage is 1.19 V and the ripple is 14 mV. The output voltage ripple has been reduced by 5 times when compared to the SC buck converter output voltage ripple of 90 mV. The efficiency of the integrated system is 63% at 1 mA load current.
Figure 3.22: Simulated waveforms of the Integrated System
Chapter 4

EXPERIMENTAL RESULTS

The layouts of our integrated power management system are discussed in this chapter. The test setup and the hardware measurement results are also presented.

4.1 Layout

The layout of the chip is shown in Fig. 4.1. It consists of a closed system which has all the blocks of the integrated system and an open system in which all blocks are laid out individually.

The layout of the switched capacitor (SC) buck converter is shown in Fig. 4.2. The SC buck converter has two capacitors of 100pF. The first capacitor of 100pF was laid out using poly1 and poly2. An NMOS transistor MOSCap is used for the layout of the second capacitor instead of poly, as we can save area. And only 50pF of the second capacitor is laid out because of the extra capacitance added by the pin package and test setup. The area of the SC converter is approximately 356 x 518 $\mu m^2$.

The layout of the clock generator is shown in Fig. 4.3. The total area of the non-overlapping clock generator is approximately 100 x 56$\mu m^2$.

The layout of the clocked comparator is shown in Fig. 4.4. The total area of the clocked comparator is around 32 x 56$\mu m^2$.

The layout of the bandgap reference circuit is shown in Fig. 4.5. The buffer used at the output of the reference circuit is also laid out. The total area of the clocked comparator is approximately 495 x 266$\mu m^2$. 
The layout of the LDO circuit is shown in Fig. 4.6. A technique called strapping was used to layout the huge pass transistor. The total area of the LDO is approximately $410 \times 390 \mu m^2$.

4.2 Test Apparatus

The procedure for testing all the blocks of the integrated system is described in Appendix A. The equipment used for testing all the blocks is given below.

1. DC Power Supply: Agilent : E3631A: 0-6V, 5A, 0-25V, 1A triple output DC power supply.


4.3 Hardware Results

The chip is fabricated in the 0.5-micron ONSEMI process through MOSIS. The chip is tested on a breadboard. A supply voltage of 3.3V is used as the system
input voltage. The system clock has a frequency of 15MHz, 3.3 Vp-p with a 1.65V offset.

4.3.1 Clock Generator

The input of the clock generator is a 15 MHz clock with fast rise and fall times. The three clock outputs are shown in Fig. 4.7. The measured dead time between the clocks was about 2 ns. The waveforms do not look square due to high operating frequency (15 MHz) on a breadboard. Testing with a custom printed-circuit board (PCB) would result in smoother recorded waveforms.

4.3.2 SC buck converter

The breadboard and 1x probe attached to the oscilloscope were adding a capacitance of about 100pF, for a total grounded capacitance of 150pF, if we include the on-chip 50pF MOSCap. The output voltage waveform is shown in Fig. 4.8. The average output voltage is 1.334V and the ripple was about 92 mV at 1 mA load current.
The average output voltage is about 70mV less than the simulated value. On the other hand, measured output voltage ripple is within 5 mV of the simulated value. But there was a capacitance of 100pF added due to the breadboard and 1x probe. Also there is a significant difference in the efficiency, due to the decrease in average output voltage.

4.3.3 Clocked Comparator

An individual clocked comparator was laid out for testing purposes. One input of the comparator was given to a reference voltage of 1.2 V. A pulse of
Figure 4.7: Measured Waveforms of Clock Generator

Figure 4.8: Measured Waveforms of SC buck converter

Average = 1.332 V
Ripple = 87 mV
frequency 7.5MHz, average value 1.22 V and 100mV<sub>p−p</sub> was given to other input. The comparator output waveform is shown in Fig. 4.9.

![Comparator Output Waveform](image)

Figure 4.9: Measured Waveforms of Clocked Comparator

### 4.3.4 Bandgap Reference

The bandgap reference circuit was tested with an input voltage of 3.3 V. The output reference voltage was about 1.25 V. And the bias current generated for the LDO was exactly 40nA. The Table 4.1 shows the variations of the bandgap reference voltage with changes in input voltage.

<table>
<thead>
<tr>
<th>Input Voltage(V)</th>
<th>Output Reference Voltage (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.000</td>
<td>1.253</td>
</tr>
<tr>
<td>3.300</td>
<td>1.2580</td>
</tr>
<tr>
<td>3.600</td>
<td>1.2597</td>
</tr>
</tbody>
</table>
4.3.5 Integrated System

The integrated system which has all the blocks was tested with an input voltage of 3.3 V and a clock of frequency 15 MHz.

![Waveform Graphs]

Figure 4.10: Measured Waveforms of Integrated System

Fig. 4.10 shows the measured waveforms of the integrated system. Average of the final output voltage at the LDO is 1.198 V. And the output voltage ripple is 33 mV compared to the SC buck converter output voltage ripple of 65 mV. The measured efficiency is about 47%.
Chapter 5

DISCUSSION AND CONCLUSION

Comparison of simulated and measured results is done in this chapter. Issues that we faced and also future work and enhancements that can be done are discussed.

5.1 Analysis of Simulated and Measured Results

Table 5.1 shows the simulated and measured results of the various blocks present in the system. The generated bandgap reference voltage is constant even with variations in the input voltage. Its temperature sensitivity was not tested. The comparator laid out individually was tested and it was able to detect time varying input signals which have a 50 mV difference.

The simulated and measured results of the SC buck converter are shown in Table 5.2. The measured average output voltage of the SC buck converter is 70 mV less than the simulated value. Also the efficiency of the SC buck converter had a big difference between the measured and simulated values.

The integrated system which includes all the blocks was also tested with a single input voltage and a system clock, and the results are shown in Table 5.3. The output voltage ripple is about 33 mV. The measured efficiency of the integrated system has a difference of 15% from the simulated value.

The flying capacitor in the switched capacitor buck converter was laid out using poly1 and poly2 materials. There is a large aparasitic capacitance added from the poly1 side to the substrate. The ratio of the poly1-to-poly2
Table 5.1: Comparison of Simulation and Measured Results

<table>
<thead>
<tr>
<th></th>
<th>Simulation</th>
<th>Measured</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Non-overlapping Clock Generator</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Deadtime</td>
<td>1.5 ns</td>
<td>2.5 ns</td>
</tr>
<tr>
<td><strong>Bandgap Reference</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{ref}$</td>
<td>1.198 V</td>
<td>1.253 V</td>
</tr>
<tr>
<td>$I_{bias}$</td>
<td>40 nA</td>
<td>39.9 nA</td>
</tr>
<tr>
<td><strong>Low Drop-out Voltage Regulator</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$Drop – out$</td>
<td>130 mV</td>
<td>170 mV</td>
</tr>
</tbody>
</table>

Table 5.2: Switched Capacitor Buck Converter Measured Results

<table>
<thead>
<tr>
<th></th>
<th>Simulation</th>
<th>Measured</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{in}$</td>
<td>3.3V</td>
<td>3.3V</td>
</tr>
<tr>
<td>Load Resistor</td>
<td>1.4kΩ</td>
<td>1.47kΩ</td>
</tr>
<tr>
<td>Average $V_{out}$</td>
<td>1.436V</td>
<td>1.332V</td>
</tr>
<tr>
<td>Output Ripple</td>
<td>93mV</td>
<td>87mV</td>
</tr>
<tr>
<td>Efficiency</td>
<td>75.6%</td>
<td>53%</td>
</tr>
</tbody>
</table>

capacitance to the poly1-to-substrate capacitance is approximately 998:83 in 0.5 micron process.

Therefore a parasitic capacitance of 9 pF to ground is part of the layout. Therefore, we simulated the SC buck converter with a 9 PF capacitor from one side of the flying capacitor to ground. We observed a 10% decrease in the efficiency of
Table 5.3: Integrated System Results Comparison

<table>
<thead>
<tr>
<th></th>
<th>Simulation</th>
<th>Measured</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{in}$</td>
<td>$3.3 \text{ V}$</td>
<td>$3.3 \text{ V}$</td>
</tr>
<tr>
<td>Load Current</td>
<td>$1mA$</td>
<td>$1.04mA$</td>
</tr>
<tr>
<td>SC Buck Converter Average $V_{out}$</td>
<td>$1.458 \text{ V}$</td>
<td>$1.383 \text{ V}$</td>
</tr>
<tr>
<td>SC Buck Converter Output Ripple</td>
<td>$90.8 \text{ mV}$</td>
<td>$65 \text{ mV}$</td>
</tr>
<tr>
<td>LDO Average $V_{out}$</td>
<td>$1.19 \text{ V}$</td>
<td>$1.98 \text{ V}$</td>
</tr>
<tr>
<td>LDO Output Ripple</td>
<td>$13.8 \text{ mV}$</td>
<td>$33 \text{ mV}$</td>
</tr>
<tr>
<td>Efficiency</td>
<td>$62.3%$</td>
<td>$47%$</td>
</tr>
</tbody>
</table>

the buck converter down to 66% with the addition of the 9 pF capacitor. However the new simulated value of 66% is still much higher than the measured efficiency of 53%.

One method to decrease the effect of the bottom plate parasitic capacitance is to layout the capacitor in an n-well and leave the n-well floating as shown in Fig. 5.1. By doing this there will be two parasitic capacitors in series. One capacitor is from poly1 to the n-well and the other from the n-well to the substrate. This adds only 4% extra parasitic capacitance, as a series capacitor is created from n-well to substrate. Now the ratio of the poly1-to-poly2 capacitance to the poly1-to-substrate capacitance becomes 998:43.

Another issue was a difference of about 100 mV in the average output voltage of the switched capacitor buck converter between the simulated and measured results. Part of this error can be explained by the omission of the 9 pF parasitic
 capaci\textit{tance}. The average output voltage with the 9 pF capacitor drops to 1.401 V. Still 70 mV remains unaccounted for.

We also had some issues while testing our circuit on a breadboard. Capacitance of about 100 pF was added due to the breadboard with 1x probe connected to the digitizing oscilloscope. Therefore testing the chip on a printed board circuit will produce better results, because there would be less stray capacitance.

While calculating the efficiency we placed a resistor in series with the input voltage source to find the average current. This series resistor introduced ripple in the input voltage of about 20mV.

\textbf{5.2 Future Work}

The switched capacitor buck converter can be improved using different methods.

\textbf{5.2.1 Time Interleaving}

A method called time-interleaving, as shown in Fig. 5.4 where two set of clocks are used to reduce the output voltage ripple. The flying capacitor is split in half. The output voltage ripple will be reduced, as it is the average of two waveforms $V_{con1}$ and $V_{con2}$. 

\begin{figure}[h]
\centering
\includegraphics[width=0.8\textwidth]{bottom_plate_capacitance.png}
\caption{Bottom Plate Capacitance}
\end{figure}
5.2.2 Capacitor Banks

Using a capacitor bank is another method that can be used to operate the switched capacitor circuit at wide range of load currents. We need to have different banks of capacitors with different capacitor values and different switch sizes. And also we need to have a sensing mechanism which switches between different capacitor banks, for different load currents. We can operate over 3 orders of magnitude in load currents by using capacitor bank over 2 orders of magnitude. Efficiency at low load currents is improved.

Different conversions ratios can be achieved in a single switched capacitor circuit using a programmable switching method.

5.2.3 Control Loop

A lot of work can be done in the controller design. In particular a voltage controlled oscillator (VCO) can be used in the feedback loop to achieve continuous frequency control of the output voltage. The output voltage ripple will be lower compared to the burst-mode pulse frequency modulation scheme.
Figure 5.3: Capacitor Banks

Figure 5.4: Implementing a VCO in PFM control loop
APPENDICES
APPENDIX A

Test Document
Supply voltages and currents:

- VDD = 3.3 V
- VSS = 0 v
- Ibias = 40 nA.

TEST PROCEDURE:

1. Connect VDD (pin 5) to 3.3V.
2. Also connect pin4(vss_pad), pin2(vss_main_os), pin17(vss_cmp), pin22(Vss_Ldo_os), pin28(Vss_ref_os), pin30(Vss_main_cs), pin34(Vss_pad), pin 37 (Vss_LD0_cs) to ground.
3. Now check whether the chip is good or fired up.

Testing the clock signals:

1. Connect Vdd_main_os (pin 3) to VDD. PIN 3 gives the Vdd supply to the clock generator and the buck converter in the open system.
2. Connect clk_gate (pin 9) to vdd (i.e high level) for now, which is one of the inputs for the AND gate.
3. Generate a clock of frequency 15 MHz, using function generator. (Vp-p = 3.3V, offset= 1.65V, high Z termination) and connect to scope to check whether it is right.
4. Now connect this clock to pin10 (Clk_main_os).
5. Connect pin 7(S1) to the oscilloscope and observe the generated clock. It must be similar to the input clock that we have generated before.
6. Connect pin 8 (S1_B) to the scope and overlap it with S1. It must be exact opposite to the S1 with no dead time in between.
7. Now disconnect the pin8 and connect pin 6 to the scope to observe S2. If we overlap S1 and S2 they must opposite to each other and must have some dead time of about 1-10 ns in between.
8. We can use 1x probe for the measurements above.
Testing the Buck Converter:

1. Connect the pin 1 to a capacitor of value 23pF (50-27). And connect the other end of the capacitor to ground.

2. Now to observe the converter output we have to generate different load currents using different resistor values. The resistor values are calculated based on the average output voltage at the output.

<table>
<thead>
<tr>
<th>LOAD CURRENT</th>
<th>RESISTOR (ohms)</th>
<th>Output Ripple</th>
<th>Average output voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 mA</td>
<td>1.4 K</td>
<td></td>
<td></td>
</tr>
<tr>
<td>500 µA</td>
<td>3 K</td>
<td></td>
<td></td>
</tr>
<tr>
<td>250 µA</td>
<td>6.2 k</td>
<td></td>
<td></td>
</tr>
<tr>
<td>100 µA</td>
<td>11 k</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10 µA</td>
<td>110 K</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

3. 110k resistor was used instead of 100k because of the 1M resistance provided in parallel by the scope.

4. Connect these resistors to pin 1 one after the other. The other end of the resistors goes to VSS.

5. Now observe the output voltage of the converter through the scope for different values of load currents. Also measure the ripple, average output voltage and tabulate the results. And save the waveforms.

6. After taking the measurements detach the resistor from the pin 1.
Testing the comparator:

1. Connect pin 19 (vdd_cmp) to VDD. This pin gives the vdd supply for both the comparators. Also connect a capacitor of value 10µF from VDD to ground.

2. Connect pin 18 (Clk_cmp) to clock with 0-3.3 V peak-to-peak and frequency of 15 MHz. We can use the clock generated above.

3. Connect pin 11 (vin_minus) to a DC voltage source of 1.2 V.

4. We must generate clock which goes from 1.25 V to 1.35 V at a frequency of 7.5 MHz. This clock can be generated by a divide by 2 circuit as shown in figure.

5. After generating a divide by 2 clock, it is given to a resistor divider circuit. The other end of the resistor divider circuit is given to the 1.2 V DC supply. The output clock of this divider circuit has a frequency of 15 MHz and goes from 1.15 V to 1.25 V. Connect this output the oscilloscope and verify it before connecting it to pin 12.

6. Connect pin 13 (Vout_comp) to the oscilloscope and check for the output of the comparator.

7. The output of the comparator will be a pulse which goes from 0 to 3.3V p-p depending on whether the pin 12 clock input is higher or lower than the vref i.e 1.2V.
Testing the voltage reference:

1. Connect pin 29 to VDD. This pin provides VDD supply for the bandgap reference.

2. To sense reference current and voltage that are generated from the bandgap reference place LMC 6482 as shown in figure below
   • Pin 3 will be the input.
   • Connect pin 8 and pin 4 of LMC 6482 to VDD and VSS respectively.
   • Short pin 1 and pin 2 of the LMC 6482.
   • Connect the pin 1 of LMC 6482 to a DMM for measuring the current or voltage.

3. Connect pin 25 (vref_out_os) to pin 3 of LMC 6482. This is the unbuffered voltage of the bandgap reference. This voltage must be 1.2 V DC with noise added to it.

4. To observe the bias current coming from the bandgap reference, connect pin 26 to a resistor of value
   \[ R = \frac{V_{\text{drop}}}{I_{\text{bias}}} = \frac{0.4 \text{ V}}{40 \text{ nA}} = 10 \text{ M}\Omega. \]
   The other of the resistor goes to VSS.

5. Disconnect pin 25 and connect pin 26 to the pin 3 of LMC 6482 and measure the current
6. Connect pin 27 to the DMM to observe the buffered reference voltage. The output voltage must 1.2V DC.

7. Detach pin 26 from the Rsense and LMC 6482 and also pin 25 from LMC6482.

**Testing the LDO:**

1. Connect pin 22 to vss supply. This pin is the vss for LDO in the open system.
2. To generate the bias current for LDO. Place a resistor of value
   \[
   R_{bias} = \frac{V_{dd} - V_{gs}}{I_{bias}} = \frac{3.3 - 0.63}{40\,\mu A} = 66\,\text{MΩ}.
   \]
   Connect one end of the resistor to VDD and other end to pin 21.
   \[R(66\,\Omega) = 10M+10M+10M+10M+10M+4.8M+1.2M\]
3. Connect pin 20 (vref_ldo) to 1.2 V DC supply, which is our reference voltage.
4. Connect pin 24(vs_ldo) to 1.5 V DC supply, as our average converter output voltage is 1.5 V and is input to the LDO.
5. To observe the output voltage

Place an IC CA 3046 and connect it as shown in the figure above, so that it forms a current mirror:

- Connect pins 9 and 12 together, so that the gates of the BJT’s are connected together.
- Connect the pins 9 & 11. This forms the diode connected BJT.
- If we want to generate a load current, connect a resistor $R_{load}$ to the pin 11. The other end of the resistor to the power supply $V_{DD}$. The resistor value is calculated as followed

$$R = \frac{V_{dd} - V_{bjt}}{I_{load}}$$

- To sense the above generated current we need to place sensing resistors $R_{sense}$ at the bottom of the mirror. For example if we have to sense a current of 0.25 mA place a resistor of 1kohm at pin 13 so that the drop across the resistor is a 250 mV and it is easily detectable. The other end of these resistors must go to $V_{SS}$.

Now connect the pin 14 of the main IC to the pin 1 of CA 3046 and the oscilloscope to observe the output voltage.

6. Also connect a capacitor of value 73 pF (100-27) to pin 23.

7. Now calculate the resistor values for different load currents using the equation above and observe output voltage ripple and average output ripple for different load currents.

8. After tabulating the results disconnect the voltage supplies at pin 24 and pin 20. Also disconnect the resistor at pin 21.

9. Detach pin 21 from $R_{bias}$ and also pins 24 and 20 from the power supplies.
CONNECTING THE OPEN SYSTEM TOGETHER:

1. Connect the pin 1 (vout_main_os) to the pin 24 (Vs_LDO_os). Keep the capacitor as it is at pin1. This connects the output of the converter to the input of the LDO in the open system.
2. Also connect the pin 1 to pin 15 (Vin_div). This connects the output of the converter to the resistor divider input.
3. Disconnect the resistor at pin 21 (Ib_LDO) and connect it to the pin 26 (Ib_out_ref). This provides the reference current for the LDO.
4. Connect pin 20 (Vref_LDO) to pin 25 (Vref_out_os) which supplies the reference voltage to the LDO.
5. Connect pin 27 (Vref_buff_os) to pin 16 (Vin_minus_comp_os). This connects the negative input of the comparator to the buffered reference voltage.
6. Disconnect pin 9 from VDD and connect it to the pin 14 (vout_comp_os). This connects the output of the comparator to one of the AND gate inputs.
7. Now observe the output voltage at both pin1 and pin 23 through oscilloscope.

TESTING THE CLOSED SYSTEM:

1. Connect pin 31 (Vdd_main_cs) and pin 40 (Vdd_ref_cs) to Vdd.
2. Connect pin 33 (CLK_main_cs) to a clock of 15 MHz generated from the function generator.
3. Connect pin 38 (Vref_cs) to pin 3 of LMC6482 as shown in the figure. The output of the LMC6482 is connected to DMM to check whether we have enough reference voltage.
4. Connect pin 32 to a capacitor of value 27 pF. Also connect it to the oscilloscope to observe the output voltage.
5. Connect pin 36 (Vout_ldo_cs) to a capacitor of value 77 pF also connect it to the pin 14 of CA 3046. And observe the voltage by connecting it to the oscilloscope.
6. Vary the load current by varying the resistor $R_{load}$ and tabulate the results.

<table>
<thead>
<tr>
<th>Load current (mA)</th>
<th>Average output voltage</th>
<th>Output ripple</th>
<th>Input power</th>
<th>Output power</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

7. To measure the efficiency
   - For the input power we placed a 60 $\Omega$ resistor in series with the input voltage to find the average input current. The input voltage is increased to 3.4 V as there is a drop of 100mv across the resistor.
     \[
     I_{in\_avg} = \frac{\Delta V}{R} \\
     \text{Pin} = I_{in\_avg} \times V_{in}
     \]
   - To find the output power, as we place a resistor at the output
     \[
     P_{out} = V_{out\_avg} \times \frac{\Delta V}{R}
     \]
   - Efficiency $= \frac{P_{out}}{\text{Pin}}$
REFERENCES


