A 22dB PSRR Enhancement in a Two-Stage CMOS Opamp Using Tail Compensation

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Abstract—A new compensation technique known as tail compensation is applied to a two-stage CMOS operational amplifier. The compensation is established by a capacitor connected between the output node and the source node of the differential amplifier. For the selected opamp topology, tail compensation allows better performance in terms of bandwidth and power supply rejection ratio (PSRR) when compared to Miller and cascode compensation. Operational amplifiers using Miller, cascode and tail compensation were fabricated in a 0.5-µm 2P3M CMOS process. The circuits operate at a total quiescent current of 90 µA with ±1.5V power supplies. Experimental results show that tail compensation increases the unity-gain frequency by 60% and 25% and improves PSRR from the positive rail by 22 dB and 26 dB over a frequency range from 23 kHz to 3.0 MHz compared to Miller and cascode compensation, respectively.

Index Terms—Tail compensation, Miller compensation, power supply rejection ratio, two-stage opamps.

I. INTRODUCTION

Power supply rejection ratio (PSRR) often determines the performance limit of sensitive analog circuitry such as ADCs, PLLs, VCOs and LDOs [1], [2]. Indeed, whenever the supply voltage is generated by a switched-mode power supply, ripple noise is unavoidable. In portable communications devices, supply ripple may even cause stability degradation at the frequency of transmission [3].

While many existing techniques, such as Miller and cascode compensation [4]–[19], ensure stability of a closed-loop amplifier, in some circumstances they lead to poor PSRR. Referring to Fig. 1, let \( V_1 \) be the output of the first stage and \( V_{OUT} \) be the output of the second stage of a two stage CMOS opamp. Miller compensation is placed between nodes \( V_1 \) and \( V_{OUT} \) and cascode compensation between nodes \( V_Y \) and \( V_{OUT} \), where node \( V_Y \) is the source of the cascoding transistor. The gain from \( V_{DD} \) to nodes \( V_1 \) [8] and \( V_Y \) is very nearly unity, as will be demonstrated later. In this way, power supply noise is easily induced through the large compensation capacitors to the output node, resulting in the degradation of PSRR at low frequencies.

To this end, we introduce a new compensation technique called “tail” compensation which does not create a path from a node contaminated by \( V_{DD} \) noise. In this technique, as shown in Fig. 1(c), the compensating capacitor \( C_T \) is connected to the low impedance tail current node \( V_X \) of the amplifier. As will be demonstrated later, the gain from \( V_{DD} \) to \( V_X \) is very nearly zero; hence the main motivation for selecting node \( V_X \) in the compensation path. From node \( V_1 \) to node \( V_{OUT} \) power supply noise is injected through the parasitic capacitance \( C_{gd} \) in the tail compensation technique. As such, PSRR begins to degrade at moderate rather than low frequencies.

II. CMOS TWO-STAGE AMPLIFIER

The circuit implementation of a two-stage operational amplifier with Miller, cascode and the proposed tail compensation schemes is shown in Fig. 2. The circuit consists of two stages, a differential pair with single-ended load \( (M_1-M_8) \) and a common-source output stage \( (M_{12}-M_{13}) \). Generally, the effective transconductance of a differential amplifier equals the transconductance of differential input transistors \( M_1, M_2 \). In this case, the load of the first stage is cascode current source \( M_3-M_4 \). The current through \( M_1 \) is not mirrored to node \( V_1 \); hence, the effective transconductance of the first stage reduces to \( 0.5g_{m1} = 0.5g_{m2} \).

The current through transistor \( M_1 \) is utilized to create a feed-forward path to node \( V_{OUT} \) through mirror \( M_5-M_6 \) and transistors \( M_9-M_{12} \). The mirror formed by transistors \( M_{11}-M_{12} \) has a dimension ratio of \( 1:K \), thus giving rise to a feed-forward transconductance of \( 0.5Kg_{m1} \). In this way, the current generated through the \( M_1 \) branch is utilized for two purposes: (i) enhancing the negative going slew-rate and (ii) biasing the output stage of the amplifier. The common-source transistor \( M_{13} \) in the second stage is similarly sized \( K \) times the unit-sized PMOS transistor. Bias voltages and currents are generated by transistors \( M_{14}-M_{19} \) and resistors \( R_6 \).

A. Op-amp Gain

Let the output resistance and equivalent capacitance to ground of the first and second stages be denoted by \( R_1 \) and...
$C_1$, and $R_{OUT}$ and $C_{OUT}$, respectively. Also, let the transconductance, output resistance, gate-to-source, and gate-to-drain capacitances of an individual transistor $M_i$ be represented by $g_{mi}$, $r_{OMi}$, $C_{gsi}$ and $C_{gdi}$, respectively. Referring to Fig. 2, the gains of the first and second stages are

$$A_{V1} = -0.5g_{m2}R_1, \quad A_{V2} = -g_{m13}R_{OUT}$$  \hspace{1cm} (1)

where $R_1 = r_{OM2}||g_{m3}r_{OM3}r_{OM4} \approx r_{OM2}$ and $R_{OUT} = (r_{OM12})||R_L$. The overall gain of the two-stage amplifier, including the feed-forward path is

$$A_V = A_{V1}A_{V2} + 0.5Kg_{m1}R_{OUT}.$$  \hspace{1cm} (2)

B. Tail Compensation

The amplifier of Fig. 2 is implemented using all three compensation techniques – Miller, cascode, and tail – in order to clearly differentiate the performance of the proposed tail compensation technique. The tail compensation capacitor $C_T$ is introduced between node $V_{OUT}$ and node $V_X$, a node with a low input resistance of $(1/g_{m3})||(1/g_{m2})$. The output of the first stage is isolated from the feedback network by the current buffer [12], [13] formed by transistor $M_2$. Current feedback through $M_2$ establishes the dominant low-frequency pole at $\omega_{p1} = (R_1(C_T^2/g_{m3})R_{OUT}).$

III. SMALL SIGNAL ANALYSIS

Small-signal models of the three compensation topologies are shown in Fig. 3. Three LHP poles and two LHP zeros were derived for each topology. A summary of the equations of poles and zeros and their unity-gain frequencies ($\omega_{UGF}$) along with their approximate frequencies for each compensation network are given in Table I. These theoretical values are computed with values from a SPICE operating point analysis using 0.5-µm transistor models.

As one can observe, the dominant pole $\omega_{p1}$ in each configuration-Miller, cascode and tail-is established by compensating capacitances $C_M, C_C$ and $C_T$, respectively. The effect of the first non-dominant pole $\omega_{p2}$ is approximately nullified through careful placement of the first LHP zero $\omega_{z1}$. The second zero $\omega_{z2}$ is at very high frequencies ($f > 150$ MHz); hence, it has negligible effect on opamp stability. The non-dominant poles $\omega_{p2}$ and $\omega_{p3}$ depend on output capacitor $C_{OUT}$. Zero $\omega_{z1}$ depends only on the compensation capacitors. The non-dominant poles in Miller and cascode are real, whereas those in tail compensation are a complex pole pair with a theoretically computed damping factor $Q \approx 0.76$.

IV. POWER SUPPLY REJECTION RATIO ANALYSIS

The PSRR small signal models of the three different compensation schemes are shown in Fig. 4. The opamp is connected in a unity-gain configuration and an AC signal in series with the DC power supply voltage is placed at the $V_{DD}$ terminal. The ratio $V_{DD}/V_{OUT}$ defines PSRR.

There are several differences in the PSRR small-signal models of Fig. 4 compared to the small-signal models of Fig. 3. Since PSRR is measured in unity-gain configuration, input $V_{IN+}$ is now at ground and $V_{OUT}$ is connected to $V_{IN-}$. Looking at the first stage of Fig. 4, the effect of transistor $M_2$ on node $V_1$ is seen in resistance $r_{OM2}$ and the effect of the unity-gain feedback is through transconductance $-0.5g_{m2}V_{OUT}$. Node $V_1$ is also loaded by $C_{g13}$ to $V_{DD}$. For common-mode voltage signals, in particular $V_{DD}$, node $V_X$ is
open, since it is loaded by cascode current source $M_7-M_8$ (see Fig. 2). Therefore, whatever current enters node $V_X$ through transistor $M_1$ must circulate back through transistor $M_2$ onto node $V_1$. The current entering node $V_X$ through transistor $M_1$, $V_{DD}/r_{oM1}$, appears at node $V_1$ as a dependent current source, as shown in Fig. 4. A final difference between the two models in the first stage is that the impedance of the cascode buffer $1/g_{m3}$ in Fig. 4(a) is now attached to $V_{DD}$.

Differences in the second stage of the PSRR small-signal model are that transconductance $g_{m13}$ in parallel with resistance $r_{oM13}$ now go to $V_{DD}$, rather than ground. $R'_{OUT}$ is the equivalent resistance to ground at node $V_{OUT}$, where $R_{OUT} = R'_{OUT}||r_{oM13}$. All other differences in the second stage are due to measuring PSRR in unity-gain configuration, wherein $V_{IN+}$ is tied to ground and $V_{OUT}$ to $V_{IN-}$.

As mentioned earlier, the reason for degraded PSRR performance in Miller and cascode compensation techniques is that noise from $V_{DD}$ appears unattenuated at nodes $V_1$ and $V_Y$. Small-signal analysis of the PSRR models in Fig. 4 yield the following gain equations from $V_{DD}$ to nodes $V_1$, $V_Y$, and $V_X$.

$$\frac{V_1}{V_{DD}} \approx 1 + \frac{1}{g_{m13}r_{oM13}} \approx 1, \quad \frac{V_Y}{V_{DD}} \approx 1$$

$$\frac{V_{DD}}{V_{DD}} \approx \frac{1}{g_{m2}r_{oM13}(K + r_{oM2}g_{m13})}$$

Using small-signal parameters, the gain $V_X/V_{DD} \approx 2.5 \times 10^{-4}$, which is close to 0.

The PSRR at low frequencies, $PSRR_{DC}$, is the same for Miller, cascode and tail compensation, and is given by

$$PSRR_{DC} = 0.5g_{m2}r_{oM2}g_{m13}r_{oM13}$$

The dominant pole determines the shape of the PSRR frequency response, which is a single-pole system for frequencies below the unity-gain frequency $f_{UGF}$. A summary of the dominant pole equations are shown in Table II. In Miller and cascode compensation, the dominant poles are created by capacitors $C_M$ and $C_C$, with theoretically computed values of 1.5 kHz and 1.2 kHz, respectively. However, in tail compensation the dominant pole is caused by the small parasitic capacitance $C_{gd13}$ of transistor $M_{13}$ and not the large compensation capacitor $C_T$. This leads to the dominant pole occurring at the moderate frequency of 23 kHz, leading to a higher PSRR for moderate-to-high frequencies.

V. EXPERIMENTAL RESULTS AND CONCLUSIONS

The three designs were implemented in a 0.5-µm 2P3M CMOS process. A chip micrograph is shown Fig. 5. Measurements were performed using power supplies ±1.5V and a total bias current of 90 µA. The output load consisted of a 40 kΩ resistor in parallel with a 20 pF capacitor. Simulated open-loop gain for all three schemes was 69 dB. To achieve a phase margin of 63°, the required compensation capacitors $C_M$, $C_C$ and $C_T$ were 1.25 pF, 1.55 pF and 2.75 pF, respectively.
of Miller and cascode compensation designs, respectively. In compensation is 22 dB and 26 dB higher, compared to that of frequencies. The PSRR of the two-stage opamp with tail best for sustained high values of PSRR over a wide range three designs. On the other hand, tail compensation proved for frequencies in the range of 23 kHz to 3 MHz. Dominant responses. The tail compensated design outperforms the Miller amplifier as a voltage follower and adding a (offset added for visibility).

While the Miller and cascode compensated designs achieved improvement of 60% over Miller and 25% over cascode. Measured transient waveforms of the amplifiers in an inverting configuration with a gain of $-1 V/V$ are shown in Fig. 6. Amplifiers are in a unity-gain inverting configuration. (Offset added for visibility).

PSRR was experimentally verified by configuring the amplifier as a voltage follower and adding a 100 mV pk−pk sinusoid to the $V_{DD}$ rail. Fig. 7 shows the measured PSRR responses. The tail compensated design outperforms the Miller and cascode compensated designs by approximately 22 dB for frequencies in the range of 23 kHz to 3 MHz. Dominant poles for PSRR for the three compensation networks closely correlate with the analytical values computed in Table II.

All hardware measurement results are summarized in Table III. The measured slew-rate performance is similar for all three designs. On the other hand, tail compensation proved best for sustained high values of PSRR over a wide range of frequencies. The PSRR of the two-stage opamp with tail compensation is 22 dB and 26 dB higher, compared to that of Miller and cascode compensation designs, respectively. In supply noise sensitive analog applications, tail compensation may prove beneficial, due to its increased $f_{UGF}$ and enhanced PSRR performance.

<table>
<thead>
<tr>
<th>TABLE III</th>
<th>SUMMARY OF MEASURED RESULTS</th>
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<tbody>
<tr>
<td>Parameter/Design</td>
<td>Miller</td>
</tr>
<tr>
<td>$f_{UGF}$ (MHz)</td>
<td>6.4</td>
</tr>
<tr>
<td>SR+SR− (V/µs) (10%−90%)</td>
<td>6.3/2.9</td>
</tr>
<tr>
<td>$PSRR @ 100$ kHz (dB)</td>
<td>44</td>
</tr>
<tr>
<td>$PSRR @ 3$ MHz (dB)</td>
<td>14</td>
</tr>
<tr>
<td>Circuit area ($µm \times µm$)</td>
<td>177 x 74</td>
</tr>
</tbody>
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REFERENCES


