A Low-Voltage, Adaptive CMOS Centroid Image Sensor with Improved Bandwidth

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Abstract—Conventional centroid architectures employ an image sensor sampled at high frame rates, analog-to-digital conversion, and digital signal processing to compute the image centroid. Latency and/or power dissipation may become prohibitively large. Therefore, fast single-chip centroid computation circuits are gaining importance in adaptive optics applications. To this end we present a fully-integrated centroid computation sensor with improved bandwidth using a transimpedance amplifier with a novel adaptive pole tracking technique. The circuit is designed to operate over five orders of magnitude of light intensity. The outputs are two signals representing the \((x, y)\) centroid coordinates of the image. A novel adaptive pole tracking technique improves the bandwidth of the sensor by approximately six times compared to the sensor in [3] with significantly reduced power consumption compared to the sensor in [4].

I. INTRODUCTION

Adaptive optics are used in applications such as target tracking, image stabilization, sun attitude detection, and free-space optical communication. These applications generally require a sensor to compute the centroid of an image. The centroid is equivalent to the center of mass of the image incident on a pixel array [1], computed as:

\[
C_x = \frac{\sum_x xI_{x,y}}{\sum_x I_{x,y}}, \quad C_y = \frac{\sum_y yI_{x,y}}{\sum_y I_{x,y}}
\]

(1)

where \(I_{x,y}\) is the light intensity at position \((x, y)\), and \(C_x, C_y\) are the horizontal and vertical positions, respectively.

In a conventional centroid system, an entire two-dimensional frame is captured by a high-speed CCD or CMOS image sensor and digitized. The data is stored and then (1) is applied to compute \((C_x, C_y)\). This process may be either too slow or too power hungry, as the designer trades off bandwidth and power consumption [2]. Hence the need for a fast, low-power fully-integrated image centroid computation sensor. Fully-integrated image sensors eliminate the need for high-speed analog-to-digital conversion, memory for data storage, and digital signal processing, all of which generally slow down and/or increase system power.

A sample image stabilization system is portrayed in Fig. 1. Light from the object is subject to turbulence by the medium it passes through, such as Earth’s atmosphere. The sample image stabilization system contains a centroid computation sensor, a controller, a tip-tilt mirror and a high resolution camera. The centroid of the image is computed by the image sensor and fed to the controller. The controller determines the movement of the tip-tilt mirror in such a way as to maintain the centroid of the image at its center. In order to obtain a stable image, the movement of the mirror must be fast. The speed of the mirror depends on the update rate of the control algorithm, which in turn is limited by the bandwidth of the sensor.

The aim of this work is to realize a low-power centroid computation sensor with high bandwidth and low power. The TransImpedance Amplifiers (TIA) in the proposed work are implemented using a novel adaptive pole-tracking technique that improves the bandwidth of the sensor by approximately six times compared to the sensor in [3] with significantly reduced power consumption compared to the sensor in [4].

The architecture of the centroid computation sensor with novel TIA’s is shown in Fig. 2. The system contains a 48x48 pixel array, row and column TIA’s, comparators, binary converters, and level shifters. Each pixel contains two photodiodes, one attached to the column line, the other to the row line. Each row and column line is connected to a TIA at the periphery, the output of which is connected to an operational transconductance amplifier (OTA). All OTA column outputs are shorted, creating voltage \(v_{CX}\), which represents \(C_x\), the centroid in the \(x\)-dimension. Similarly, OTA row outputs are shorted to create \(v_{CY}, v_{CX}\), and \(v_{CY}\) are digitized to 6-bit outputs using clocked-comparators [5] and a binary converter. Level shifters allow for high-speed digital readout.
II. LOW-POWER, HIGH-BANDWIDTH ADAPTIVE TIA

Adaptation can be achieved in a number of ways. For example, Basu et al increase the bias current of the first stage [6]. A complex method of adaptation using smooth pole tracking was implemented by Wong and Evans [7] for use in low-dropout voltage regulators. This paper discusses a novel method of adapting pole locations in a TIA without incurring higher quiescent power consumption. Adaptation is achieved by making use of the body-effect on the output stage PMOS transistor.

A. Circuit Design

The proposed TIA is designed as a three-stage amplifier, as shown in Fig. 3. The output stage is a PMOS transistor, which operates as a common-source amplifier. This stage is biased with photocurrent. Due to the large parasitic capacitance associated with the photodiodes tied to this node (several pF), the output pole is dominant. The second stage is a conventional common-source amplifier with a current source load. The capacitance associated with this node is small, and hence, this is the non-dominant pole. The first stage is a common-source amplifier with diode-connected load. This stage provides the phase-shift required for the circuit to be a negative-feedback system.

The body terminal of transistor $M_5$ in Fig. 3 is set to a potential greater than its source voltage. This causes the PMOS to be body-effected, so that $|V_{TH,P}|$ is large. The amount of back-gate voltage required can be estimated from the point at which adaptation should occur.

The overdrive voltage of transistor $M_2$ is set to 350 mV. When the circuit functions without the adaptive effect at low illumination levels, the voltage $V_{TH,A}$ will be greater than the overdrive voltage of $M_2$, placing $M_2$ in saturation. In this mode, the two poles are far from each other and hence no adaptation is required. The voltage gain of the first two stages is

$$A_V = g_{m1} \left( \frac{1}{g_{m3}} \right) g_{m4} \left( r_{o2} \right) \left( r_{o4} \right),$$

(2)

$A_V$ determines the amount of bandwidth enhancement of the system.

When illumination levels reach the point of adaptation, the voltage $V_{TH,A}$ will be less than or equal to 350 mV. Thus, transistor $M_2$, which was in saturation, is pushed into triode. At the point of adaptation, the gain provided by the second stage amplifier reduces smoothly because the NMOS load on the second stage now behaves as a resistor instead of a current source. As a result, the non-dominant pole is moved out to higher frequencies because the resistance at that node is $(r_{o4}|r_{o2})$ instead of $(r_{o2}|r_{o4})$. This change in load decreases the voltage gain of the first two stages, $A_V$. This adaptation technique allows the TIA to achieve high gain at low illumination levels, while ensuring stability at high illumination levels.

B. Small-Signal Analysis

In Fig. 4, the closed-loop small-signal model of the proposed TIA is presented. The first two stages are combined to generate an in-phase transconductance gain parameter $G_{m1}$. The out-of-phase transconductance parameter $G_{m2}$ corresponds to the third (output) stage. Resistors $R_1$ and $R_2$ correspond to the output resistances of the first two stages (combined) and the third stage, respectively. $C_{gd5}$ is the gate-to-drain capacitance of transistor $M_5$. Capacitance $C_1$ corresponds to the gate-to-source capacitance of transistors $M_5$, $M_6$, and $M_7$. Capacitance $C_2$ corresponds to the large parasitic photodiode capacitance. Approximate pole-zero analysis
shows:

\[
\omega'_{z1} = -\frac{G_{m1}}{C_{gd5}} \\
\omega_{p1} = -\frac{1 + G_{m1}R_1G_{m2}R_2}{R_2C_2} \\
\omega_{p2} = -\frac{1}{R_1(C_1 + C_{gd5})}
\]

Thus, we find two major poles and one left-half-plane zero.

C. High Precision Centroid Computation Sensor

A schematic of the portion of the centroid computation sensor that computes \(v_{CX}\) is shown in Fig. 5. A similar circuit is used to compute \(v_{CY}\) along each pixel row. In contrast to the centroid computation architecture of [2], an active-input current mirror is used to isolate the large photodiode capacitance \(C_{PHi}\) from the differential amplifiers. The main advantage of this scheme is increased bandwidth, as the resistance associated with \(C_{PHi}\) is \(R_{IN,i} = 1/(AVg_{m5})\), where \(AV\) is the gain of the TIA.

A second major advantage of this architecture is improved accuracy in the centroid computation through the use of linearized differential pairs. Referring to Fig. 5, the active-input current mirror \(M_{5,i} - M_{7,i}\) has two output currents labeled \(mi_{PHi}\), where \(m > 1\). These currents are input to a linearized PMOS differential pair \(M_{8,i} - M_{11,i}\), using symmetric diffusors [8], which has a linear range that is 3.5 times higher than that of a simple differential pair. Because of this linearizing technique, the resulting centroid voltage is more precise.

The non-inverting input to the differential pair is a DC voltage generated by a resistor string (not shown in Fig. 5). The inverting terminal is tied to the output. All of the output currents of the differential pairs are connected to a single cascaded NMOS current mirror \(M_{12} - M_{15}\) to complete a single-ended linearized operational transconductance amplifier (OTA). The output of this OTA is the voltage \(v_{CX}\), which represents the centroid of the image incident in the \(x\)-dimension.

In simulation, we show a six times increase in bandwidth over a simple diode-connected PMOS transistor with no transimpedance amplifier, which has a similar bandwidth to that found in [2]. From Fig. 6 we see the TIA operates without adaptation up to a photocurrent of 700 nA. At this point, the TIA adapts to a low gain region. As such, the bandwidth flattens out and then decreases to merge with the curve of the diode-connected PMOS transistor.

III. EXPERIMENTAL RESULTS

A two-dimensional 48x48 array centroid computation sensor is designed and fabricated in a 0.5-\(\mu\)m 2P3M CMOS process. The system operates with a single supply voltage of 1.8 V. Bias voltages \(V_{BH}\) and \(V_{BN}\) are 300 mV and 900 mV, respectively. The size of each pixel is 20.25x20.25 \(\mu\)m\(^2\), with a fill-factor of 97%. Each pixel contains two photodiodes that generate photocurrents for the \(x\)- and \(y\)-dimension centroid computation circuits. The total bias current \(I_b\) of each TIA is 2 \(\mu\)A, which is more than 10 times lower than the 22 \(\mu\)A bias current of the TIA introduced in [4]. A micrograph of the proposed centroid computation sensor is shown in Fig. 7.

Static measurements of the centroid voltage are done by focusing a He-Ne laser beam on a specific pixel and moving
it across the array. The results of these measurement are shown in Fig. 8. It is observed that the measured position-encoded voltage levels are very close to simulated values. The plot also shows monotonicity over all the three chip measurements, which is vital for gradient search control algorithms.

Dynamic measurements are done with two super bright LEDs, which are driven out-of-phase. The output voltages are plotted on the oscilloscope and measured using the digital multimeter (DMM). The shape of the waveform on the oscilloscope is sinusoidal if the chip is tracking both light sources correctly. Dynamic measurements are used to measure the bandwidth of the system as a function of photocurrent, which is proportional to light intensity. Fig. 9 is a plot comparing the simulated bandwidth vs. photocurrent curve and the measured curve. Measurements above photocurrents of 100 nA were not achievable with our experimental setup.

**IV. DISCUSSION AND CONCLUSION**

The proposed centroid computation sensor is compared with three sensors from the literature. The measured results are summarized in Table I. The proposed 48x48 sensor array is designed with a pitch of 20.25x20.25 µm² and the total area of the microchip is 2.18 mm². It operates with a 1.8 V supply and consumes only 2.16 mW. The bandwidth of the sensor is much higher than the sensors presented in [2] and [3] and almost equal to that of the sensor presented in [4]. However, the total power consumed is approximately 40% lower than the sensor in [4], despite the fact that the proposed sensor array size is 44% larger. As such, the proposed fully-integrated CMOS centroid image sensor is suited to adaptive optics systems where high speed, small size and low power consumption are required.

**Table I**

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Process (µm)</td>
<td>2</td>
<td>0.5</td>
<td>0.5</td>
<td>0.5</td>
</tr>
<tr>
<td>Supply (V)</td>
<td>3.2 ±1.25</td>
<td>±0.9</td>
<td>1.8</td>
<td></td>
</tr>
<tr>
<td>Power (mW)</td>
<td>3.74</td>
<td>2.16</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Array Size</td>
<td>160x160</td>
<td>1x7</td>
<td>40x40</td>
<td>48x48</td>
</tr>
<tr>
<td>Pixel Area (µm²)</td>
<td>43x43</td>
<td>20x20</td>
<td>20x20</td>
<td>20x20</td>
</tr>
<tr>
<td>Chip Area (mm²)</td>
<td>46.9</td>
<td>0.07</td>
<td>2.18</td>
<td></td>
</tr>
<tr>
<td>$f_{3dB@i_{PH}=1nA}$ (kHz)</td>
<td>8</td>
<td>6.5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$f_{3dB@i_{PH}=10nA}$ (kHz)</td>
<td>55</td>
<td>50</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$f_{3dB@i_{PH}=100nA}$ (kHz)</td>
<td>55</td>
<td>100</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**REFERENCES**


