Chapter 4 – The Active and Poly Layers

E E 480 – Introduction to Analog and Digital VLSI
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Wires are routed over the FOX (field oxide)
Transistors (MOSFETs) fabricated in the openings in the FOX

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- Active layer also called diffusion layer
- By hand, we will draw either p+ or n+ layer.

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p+ is the intersection of active and p-select (RX and BP layers in 130nm process)
n+ is the intersection of active and n-select (RX and absence of BP layer in 130nm process)
Field oxide will be placed under the gate (poly), making the "transistor" useless

Thin oxide is required under the gate

In CMOS self-aligned process, thin oxide and then poly gate is placed on the substrate.

Then B or P ions are implanted in the active area and the gate (to make p+ or n-active)

Gate blocks the B or P ions from reaching the substrate, so source/drain regions align perfectly.

Relative doping levels:
- $n^{++}$ poly gate ~ $1 \times 10^{21}$ atoms/cm$^3$
- $n+$ or $p+$ active ~ $1 \times 10^{19}$ atoms/cm$^3$

Silicide is a mixture of polysilicon and tungsten

Thin layer placed on top of silicon and active areas (after transistors are formed) to reduce the sheet resistance of poly (and active)

Poly (+silicide) used for short-length wiring
Table 4.1 Typical properties of resistive materials in a CMOS process.

| Sili-cide | Resistor Type | $R_{\text{sheet}}$ (ohms/sq.) | TCRI | TCRI | TCRI | TCRI | TCRI | Mis- |
|-----------|---------------|------------------------------|------|------|------|------|------|------|------|
|           |               | (Vppm/C) | AVG. | (Vppm/C) | AVG. | (Vppm/C) | AVG. | (Vppm/C) | AVG. | (Vppm/%) | AVG. | (Vppm/%) | AVG. |
| N/A       | well          | 500 ± 10 | 2400 ± 50 | 7 ± 0.5 | 8000 ± 200 | 500 ± 50 | < 0.1 |
| No        | n++ poly      | 200 ± 1  | 20 ± 10  | 0.6 ± 0.03 | 700 ± 50 | 150 ± 15 | < 0.5 |
| No        | p++ poly      | 400 ± 5  | 160 ± 10 | 0.8 ± 0.03 | 900 ± 50 | 150 ± 15 | < 0.2 |
| No        | n+            | 100 ± 2  | 1500 ± 10 | 0.04 ± 0.1 | 2500 ± 50 | 350 ± 20 | < 0.4 |
| No        | p+            | 125 ± 3  | 1400 ± 20 | 0.4 ± 0.1 | 80 ± 80  | 100 ± 25 | < 0.6 |
| Yes       | n++ poly      | 5 ± 0.3  | 5500 ± 90 | 1.0 ± 0.2 | 2500 ± 125 | 3800 ± 400 | < 0.4 |
| Yes       | p++ poly      | 7 ± 0.1  | 3600 ± 50 | 1.0 ± 0.2 | 2500 ± 100 | 5500 ± 250 | < 0.7 |
| Yes       | n+            | 10 ± 0.1 | 3700 ± 50 | 1.0 ± 0.2 | 350 ± 150 | 650 ± 60  | < 1.0 |
| Yes       | p+            | 20 ± 0.1 | 3800 ± 40 | 1.0 ± 0.2 | 150 ± 50  | 800 ± 40  | < 1.0 |

- n++ poly with no silicide has $R_{\text{sheet}} = 200 \ \Omega/\square$
- n++ poly with silicide, $R_{\text{sheet}} = 5 \ \Omega/\square$
- M1, $R_{\text{sheet}} = 0.1 \ \Omega/\square$

Silicide is placed over all n+, p+ and poly regions.

- If you want to create a high-resistance poly resistor (e.g., 1 kΩ to 10 MΩ), add silicide block to increase the sheet resistance.
- With or without silicide $C_{\text{poly-to-bulk}}$, the same
- Only difference $R_{\text{sheet}}$ 20x smaller with silicide
- Distributed $R$ and $C$, so $t_d = 0.35 R_{\text{lump}} C_{\text{lump}}$
• All contacts to poly from M1
• Poly wire over FOX (thick)
• Poly gate over thinox

Figure 4.8 How metal1 is connected to poly and active.
- All contacts from active areas to M1
- Contacts from poly to active not normally allowed
• Pins to the "real world" always on metal layer.

Figure 4.10 Layout of an n-well resistor and the corresponding cross-sectional view.

• Poly over active region = poly gate
• Thin oxide beneath poly gate
• Process named by minimum L (length) of transistors, which is the minimum width of poly.

Figure 4.12 Layout and cross-sectional views of an NMOS device.

• For PMOS, diffusions/bulks are complemented
• n-well terminal tied to Vin through n+ region

Figure 4.13 Layout and cross-sectional views of a PMOS device.

(a) NMOS device with body tied to ground.
(b) PMOS device with body tied to VDD.
(c) Bipolar-derived NMOS symbol with body tied to ground.
(d) Bipolar-derived PMOS symbol with body tied to VDD.
(e) NMOS symbol where the arrow indicates the p-substrate to n-channel diode.
(f) PMOS symbol where the arrow indicates the n-well to p-channel diode.

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• Standard Cell Layout
• VDD at top, VSS at bottom
• PMOS transistors in n-well, NMOS transistors in substrate
• Height of cells never changes

(b) Increasing the area available for layout of MOSFETs.
• Height of Standard Cells never changes
• Widths of cells varies with complexity, e.g., inverter narrower than OR
• VDD, VSS wires line up perfectly
• m-well, n-select, and p-select overlap.

Active minimum width = 1.5
Active minimum spacing = 1.5
Active minimum distance to well, 2.5
(Active used for substrate/well contact can be within 1.5 of well.)
Active extension beyond poly, 1.5
Poly minimum width, 1
Poly minimum spacing, 2
Poly to active space, 0.5
Poly gate extension over active minimum, 1.25

Contact to gate spacing, 1
Select overlap of contact minimum, 0.75
Select to poly gate distance minimum, 1.5
N-select (NMOS)
Select overlap of active minimum, 1

Figure 4.16 Design rules for active, selects, poly, and contacts.
Adding diodes to the pads to protect the MOSFET gates from ESD damage.

- If input voltage > \( V_{DD} + 0.5V \), \( D_2 \) conducts
- If input voltage < \( V_{SS} - 0.5V \), \( D_1 \) conducts
- Gate oxides will be damaged (typically shorted to channel) if voltage greatly exceeds rails

Figure 4.20 Layout of a padframe using pads with ESD diodes.

Figure 4.21 Layout used in Problem 4.2.

- Poly cross-section goes from over “thick ox” (substrate) to over “thin ox” (active) to over “thick ox” (substrate) again.