A Multi-Loop Low-Dropout FVF Voltage Regulator with Enhanced Load Regulation

BY

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A thesis submitted to the Graduate School in partial fulfillment of the requirements for the degree Master of Sciences, Engineering

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“A Multi-Loop Low-Dropout FVF Voltage Regulator with Enhanced Load Regulation,” a thesis prepared by Mahender Manda in partial fulfillment of the requirements for the degree, Master of Sciences has been approved and accepted by the following:

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DEDICATION

Dedicated to my mother Vani Manda, father Eshwaraiah Manda, sisters Yamini, Sindhuja and Razia, brother-in-law Praveen, and Knights.
I express my gratitude to Dr. Paul Furth for being my advisor. I would like to thank Dr. Furth for being an amazing teacher all these years. I would like to appreciate Dr. Furth for treating all his students as a family through out our stay at NMSU.

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ABSTRACT

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We introduce a multi-loop fast transient response flipped voltage follower (FVF) low-dropout (LDO) voltage regulator suitable for system-on-chip (SOC) applications. While typical FVF-based LDOs exhibit fast transient response, which is critical for SOC applications, their output DC accuracy is limited due to low loop gain of the FVF. In this work, we introduce a multi-loop design aimed at improving the DC accuracy while preserving the transient performance. The LDO is implemented in a 180-nm CMOS process to provide an output voltage
of 1.5 V at a maximum load current of 10 mA from an input line voltage of 1.8 V. The designed LDOs quiescent current is 53 μA at minimum load. Simulation results showcase the advantages of the multi-loop design with a transient response time of 0.73 ns and a figure of merit (FOM) of 3.9 ps.
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Chapter 1

INTRODUCTION

Expeditious advancement of science and technology in the last decade has made human life easier. We are able to see what is happening all around the world in hand-held portable electronic devices. These portable devices can be laptops, smart phones, tablets or other devices. With the increase in demand for portable electronics, system-on-chips (SOCs) with increased complexity have become widely prevalent. SOCs require several circuit blocks to implement a complete system; a Power Management Unit (PMU) is one among them. A PMU constitutes multiple DC-DC power converters, which convert the input battery voltage to different output voltages. Low-dropout (LDO) voltage regulators, inductor-based switching regulators and capacitor-based switching regulators are three types of conventional power converters.

Fig. 1.1 shows the block diagram for a wireless sensing system with power management unit included. Fig. 1.2 illustrates the components inside the PMU. This PMU has multiple DC-DC power converters to convert the battery voltage to different voltage levels which are required to drive other components in the system. It can be observed that the PMU employs three switching regulators and two LDOs. Switching regulators MAX618 and MAX765 generate +12V and -12V, respectively, to drive instrumentation amplifiers (AD620B), whereas MAX1722 generates +5V to drive the anti-aliasing filter and ADC. LDO MCP1700 sup-
plies $+5V$ to ADR341 which generates a reference voltage for the ADC. Another MCP1700 LDO is utilized to power the wireless transceiver CC1110 with $+3.3V$.

1.1 Motivation

While incorporating a power management unit on an SOC, voltage regulators which require minimal area are essential for providing necessary supply voltages for various subsystems [3], [4]. Fully integrated low-dropout voltage regu-

Figure 1.1: Block diagram of wireless sensing unit [1].

Figure 1.2: Power management unit for a wireless sensing unit [1].
lators are specifically used in such circumstances due to their off-chip component-free feature. Among many existing topologies, fully-integrated flipped voltage follower (FVF) based LDOs are an attractive topological choice for on-chip applications due to their low output impedance, fast transient characteristic and minimal area requirements [2], [5].

Despite the above mentioned advantages of FVF LDOs, they suffer from an architectural problem of poor load regulation [6]. This is not a desirable quality for an LDO, especially if it is designed to drive a digital load which alternates between sleep mode and active mode. This motivated the current research, which proposes a new technique to improve the load regulation of FVF LDOs.

1.2 Report Organization

This thesis report is organized into five chapters, where:

Chapter 2 describes the operation and performance parameters of an LDO. It also reviews the literature of FVF and FVF LDOs.

Chapter 3 presents the implementation details and simulation results of the proposed multi-loop FVF LDO. Moreover, the operation and necessity of each loop is also discussed in this chapter.

Chapter 4 shows the layout and chip-level measurement results of two different FVF LDO designs.

Chapter 5 summarizes the results and compares this work with other state-of-the-art work in the literature. It also presents issues of fabricated design and future work associated with the proposed design.
Chapter 2

LITERATURE REVIEW

A voltage regulator maintains a constant output voltage irrespective of variations in load current or supply voltage. DC-DC converters and LDOs are voltage regulators which can provide an output voltage which is different from the input voltage. DC-DC converters can step-up or step-down the input voltage level depending upon the application, whereas LDOs provide an output voltage which is always less than the input voltage.

2.1 LDO as a Voltage Regulator

An LDO comprises an error amplifier, a feedback network and a pass transistor, as shown in Fig. 2.1. A simple LDO incorporates an op-amp as an error amplifier, a resistor divider as a feedback network and a PMOS FET as pass transistor. One input for the error amplifier is the reference voltage and the other input is the scaled output voltage from the feedback network. The feedback network scales down the output voltage only when the desired output voltage is higher than the reference voltage. The error amplifier amplifies the difference between the scaled output voltage and the reference voltage. The output of the error amplifier drives the pass transistor to source the necessary amount of current to the load in order to achieve the desired output voltage.

Consider the LDO shown in Fig. 2.1. If there is a decrease in the load current during a load transient, the output voltage will increase beyond the de-
desired value. Therefore the voltage at the positive terminal of the error amplifier increases, creating a voltage difference between the input terminals. The error amplifier amplifies the difference between its input terminals thereby increasing the voltage at the gate of the pass transistor. This decreases the source-to-gate voltage of the pass transistor, reducing the current being sourced to the load, consequently returning the output voltage back to the desired value. A similar negative feedback action will take place when the output voltage decreases below the desired value due to a sudden increase in load current. Therefore an LDO can be described as a negative feedback system which adjusts the source-to-gate potential of the pass transistor to regulate the output voltage for a wide range of load currents.

2.2 Performance Parameters of an LDO

Dropout voltage, line regulation, load regulation, overshoot, undershoot and recovery time are the performance parameters discussed in this section.
2.2.1 Dropout Voltage

Dropout voltage is the input-to-output differential voltage at which the circuit ceases to regulate against further reductions in input voltage [7]. It can be understood as the minimum voltage drop across the pass transistor.

The dropout voltage of an LDO increases almost linearly with increases in the load current; therefore, the maximum dropout voltage of an LDO is seen at the maximum load current [8]. In this work, we measured the dropout voltage as the difference between input voltage and output voltage when the output voltage is 2% less than the maximum, or desired, value, that is,

$$V_{DO} \equiv (V_{IN} - V_{OUT}) \mid I_L = I_{L,MAX}, V_{OUT} = 0.98 \cdot V_{OUT,MAX}$$

(2.1)

![Figure 2.2: Dropout voltage.](image)

2.2.2 Line Regulation, Overshoot and Undershoot

This parameter indicates how well an LDO can regulate the output voltage irrespective of changes in the line voltage (input voltage). During a line transient
event, the input voltage is switched high and low with fast rise and fall times, as shown in Fig. 2.3. It can be observed from Fig. 2.3 that the output voltage shoots up when the input voltage switches high and shoots down when the input voltage switches low. When the input voltage is switched high, the difference between the peak value and the steady-state value of the output signal is defined as overshoot. Similarly, when the input voltage is switched low, the difference between the minimum value and the steady-state value is defined as undershoot.

Line regulation is the ratio of steady-state change in output voltage ($\Delta V_{OUT,SS}$) to the steady-state change in input voltage ($\Delta V_{IN,SS}$). It is defined as:

$$\text{Line Regulation} \equiv \frac{\Delta V_{OUT,SS}}{\Delta V_{IN,SS}}$$  \hfill (2.2)

It is generally expressed in units of mV/V. The total change in output voltage due to a line transient event is define as

$$\Delta V_{OUT,LINE} \equiv \Delta V_{OUT,SS} + \text{Overshoot} + \text{Undershoot}$$  \hfill (2.3)

It is the same as the maximum minus minimum voltages during a line transient event.

2.2.3 Load Regulation

This parameter indicates how well an LDO can regulate the output voltage irrespective of changes in the load current. During a load transient event, output voltage shoots down when the load current is switched high and shoots up when the load current is switched low as shown in the Fig. 2.4.
Load regulation is defined as the ratio of steady-state change in output voltage ($\Delta V_{OUT,SS}$) to the steady-state change in load current ($\Delta I_{LOAD,SS}$).

\[
\text{Load Regulation} \equiv \frac{\Delta V_{OUT,SS}}{\Delta I_{LOAD,SS}}.
\]

(2.4)

It is expressed in units mV/mA. The total change in output voltage because of a load transient event is calculated as

\[
\Delta V_{OUT,LOAD} = \Delta V_{OUT,SS} + \text{Overshoot} + \text{Undershoot}
\]

(2.5)

### 2.2.4 Recovery Time

As described in the above subsections, line and load transients will alter the output voltage, but the LDO gets back to desired output voltage after a certain
amount of time. Recovery time is the amount of time an LDO needs to set the output voltage back within the allowed tolerance band of the steady-state output voltage. In this work, we considered the output voltage is within the allowed tolerance band only when the output voltage is either 2 percent higher or lower than the final steady-state value.

Fig. 2.5 illustrates the concept of recovery time. The time taken by the LDO to get output voltage back in to the allowed tolerance band after the overshoot is denoted as $T_{RH}$ and after the undershoot is denoted as $T_{RL}$.

2.3 Voltage Follower and Variants

In this section, we describe several voltage follower circuits and qualitatively compare their characteristics.
2.3.1 Voltage Follower (Common-drain Amplifier)

The PMOS version of a common-drain amplifier is shown in Fig. 2.6. Input $V_{IN}$ is applied to the gate of transistor $M_{CD}$, while the output $V_{OUT}$ is obtained at its source terminal. Since the bias current $I_{CD}$ is always constant, the source-to-gate voltage $V_{SG}$ of $M_{CD}$ is fixed. Therefore, any small-signal change in the input will be directly followed by the output in order to keep the $V_{SG,MC}$ constant.

From Fig. 2.6 the range of the input is

$$V_{SS} \leq V_{IN,CD} \leq V_{DD} - V_{SAT,ICD} - V_{SG,MC} \quad (2.6)$$

The CD buffer has high current sinking capability whereas its sourcing capability is limited by bias current $I_{CD}$. The output impedance of the CD buffer is given by

$$R_{OUT} = 1/\text{gm}_{CD} \quad (2.7)$$
2.3.2 Flipped Voltage Follower (FVF)

The schematic of a PMOS FVF [9] is shown in Fig. 2.7. An FVF consists of a PMOS input control transistor $M_{FVF}$, transistor $M_2$ with shunt feedback and bias current $I_{FVF}$. The operation of the FVF is similar to the CD, but the FVF has high current sourcing and limited current sinking capability. The internal feedback loop helps in reducing the output impedance by the internal loop gain, which is given by

$$\text{Loop gain} = g_{m_2} \cdot r_{o_{FVF}} \quad (2.8)$$

Therefore, the output impedance of an FVF is given by

$$R_{OUT} = \frac{1}{g_{m_{MFVF}} \cdot (g_{m_2} \cdot r_{o_{FVF}})} \quad (2.9)$$

Although an FVF exhibits ultra-low output impedance, it suffers from limited operating voltage range. The input voltage range is limited by feedback transistor
$M_2$ and is given by

$$V_{DD} - V_{SG,M2} + V_{SD,MFVF} - V_{SG,MFVF} \leq V_{IN,FVF} \leq V_{DD} - V_{SD,M2} - V_{SG,MFVF}$$

(2.10)

2.3.3 Folded Flipped Voltage Follower (FFVF)

The Folded Flipped Voltage Follower (FFVF) [9] has ultra-low output impedance and does not suffer from limited operating voltage range. The PMOS version of an FFVF, shown in Fig. 2.8, contains PMOS control transistor $M_{FVF}$ and additional NMOS feedback transistor $M_2$. In order to eliminate the voltage clamping issue in the FVF, the feedback transistor is folded. This doubles the bias current required to $2I_{FVF}$, but helps in restoring the voltage range to becoming
similar to a CD stage. The input range of the FFVF is given by

$$V_{SS} + V_{SG,M2} + V_{SD,FFVF} - V_{SG,FFVF} \leq V_{IN,FFVF} \leq V_{DD} - V_{SD,2FVF} - V_{SG,FFVF}$$

(2.11)

On the other hand, $M_2$ also provides the feedback that reduces the output impedance which is similar to the FVF. So, the FFVF has ultra-low output impedance and also better input voltage range than the FVF.

![Figure 2.8: FFVF.](image)

### 2.4 FVF LDOs

Several LDOs employing FVF output stages have been published in the literature. We will review several of them.

#### 2.4.1 Single-Transistor-Control LDO

In [2], the author explains the operation of the FVF as an LDO. It is described as Single-Transistor-Control (STC) LDO because a single transistor controls the operation of the LDO. Fig. [2.9] shows the architecture of the STC LDO.
proposed in [2]. It is divided into three parts: error amplifier, $V_{SET}$ generation and the FVF stage.

![Figure 2.9: STC LDO adapted from [2].](image)

One input for the error amplifier is reference voltage $V_{REF}$ and the other is voltage fed back from node $V_{MIR}$. Therefore, $V_{MIR}$ is regulated by the error amplifier to be equal to $V_{REF}$. The $V_{SET}$ generation stage forms the bridge between $V_{MIR}$ and $V_{OUT}$. $V_{SET}$ is held one $V_{SG}$ below $V_{MIR}$ by diode-connected transistor $M_7$. Generated $V_{SET}$ acts as input for FVF LDO stage. From Fig. 2.9 it can be observed that $V_{MIR}$ and $V_{OUT}$ are equal due to the floating current mirror formed by transistors $M_7$-$M_8$.

Pass transistor $M_{PASS}$ and control transistor $M_8$ with the current source forms the FVF stage. $M_{PASS}$ is sized to be capable of maintaining sufficient dropout voltage and also to source the necessary amount of load current. The connection from the drain of the control transistor to the gate of the pass transistor closes the negative feedback loop, which regulates the output voltage.

A load transient from maximum load to minimum load causes the output voltage to increase. This increase in output voltage is sensed, amplified and fed back to the gate of $M_{PASS}$ by common-gate amplifier $M_8$. An increase in the gate
voltage will reduce the $V_{SG}$ of the pass transistor, sourcing less current to the load. This mechanism regulates the output voltage but, because of the generally low loop gain of the FVF stage, it offers poor load regulation [10].

Poor DC accuracy of the output voltage is one disadvantage associated with this architecture [6]. If the error amplifier has an input offset, it will make voltages $V_{MIR}$ and $V_{REF}$ differ slightly from each other, which in turn results in mismatch of $V_{OUT}$ and $V_{REF}$. Another issue which affects the DC accuracy of the output is the $V_{SG}$ mismatch in the floating current mirror formed by transistors $M_7$ and $M_8$. Mismatch in $V_{SG}$ of $M_7$ and $M_8$ will generate an offset between $V_{OUT}$ and $V_{MIR}$.

The author in [2] also explains the stability of the STC LDO with an off-chip output capacitor and without an output capacitor for three cases of load current: minimum, moderate and maximum. According to [2], the STC LDO has three poles and one zero. The output pole ($P_{OUT}$) and the pole at the gate of the pass transistor ($P_{GATE}$) are the two low frequency poles. The third is a high frequency pole ($P_{HF}$). The zero is formed by the ESR of the output capacitor.

With an off-chip output capacitor: for all three cases of load current, the Miller effect is not significant on $C_{GD}$ of the pass transistor and as the output capacitor is large, $P_{GATE}$ has no chance to be the dominant pole. However, $P_{GATE}$ can be cancelled by the zero and $P_{HF}$ is located after the unity-gain frequency, making the LDO stable with the output dominant pole for all the three cases of load currents.

Without output capacitor: In this situation, there is no significant capacitance at the output node, moving $P_{OUT}$ to a frequency greater than the UGF. This makes $P_{GATE}$ dominant. In general, $P_{HF}$ is located far enough from $P_{GATE}$ to make LDO stable for all the three cases of load current.
Another limitation of the STC LDO is minimum load current requirement [10]. If the load current is less than the minimum, then the gate voltage of the pass transistor has to increase in order to decrease $V_{SG}$ of the pass transistor. Increasing the gate voltage of $M_{PASS}$ will push transistor $M_8$ into triode, which is not desirable for the operation of LDO. In [10], the authors also show the stability issue at high load currents. For high load currents, the output resistance ($r_o$) of $M_{PASS}$ decreases and hence moves the output pole to high frequency, close to the pole at the gate of $M_{PASS}$. Having these two poles close to each other leads to instability. To avoid this situation, the pole at the gate of $M_{PASS}$ has to be moved to high frequency, which is possible by reducing either the capacitance or the resistance associated with the node $V_G$. However, the amount of output current governs the size of $M_{PASS}$ which in turn decides the size of the capacitor $C_{GD}$. So, the other possible way to move the pole at the gate to high frequency is to reduce the resistance at the node $V_G$.

From the discussion of the STC LDO above, we conclude that it suffers from the problems of poor load regulation, minimum load current requirement and also maximum load current limitation.

2.4.2 Buffered FVF LDO

In [10], the authors propose a buffered FVF architecture incorporating a cascoded and level-shifted FVF to overcome the problems suffered by the STC LDO. The cascoded FVF is shown in Fig. 2.10. It has an additional NMOS transistor in the feedback loop of the FVF stage. The additional transistor acts as a common-gate amplifier, offering extra gain in the feedback loop. This increases the loop gain of the FVF, providing higher load regulation than the regular FVF stage. This improved architecture holds the node $V_A$ at a constant voltage $V_{BIAS}$—
V_{SG,MCA} which will enable the transistor $M_C$ to be in saturation irrespective of the load current, thereby avoiding the minimum load current requirement.

![Cascoded FVF](image)

Figure 2.10: Cascoded FVF.

The level-shifted FVF from [10] is shown in Fig. 2.11. This design has a PMOS transistor in the feedback loop of the FVF stage. Transistor $M_{LS}$ level shifts the voltage at the node $V_A$ to $V_G - V_{SG,MLS}$ thereby reducing the problem of minimum load current. As shown in Fig. 2.11, the gate of $M_{PASS}$ is connected to the source of transistor $M_{LS}$, yielding low impedance at the node $V_G$. This moves the pole at the gate of $M_{PASS}$ to higher frequency, rectifying the limitation on high load currents.

The buffered FVF architecture of [10] is shown in Fig. 2.12. It can be observed that transistor $M_{LS}$ provides a level shift for $M_C$ to be able to stay in saturation, avoiding the problem with minimum load current. Transistor $M_{LS}$ also helps to move the pole at node $V_G$ to high frequency, relaxing the limitation on high load current. $M_{CA}$ acts as a common gate stage to improve the loop gain, offering improved load regulation compared to normal the FVF LDO.
The buffered FVF architecture discussed above has achieved three major benefits: relaxing the limitation on high load current, mitigating the problem of minimum load current and increasing the loop gain to provide improving load regulation over that of the FVF stage.
2.5 Fully-Integrated FVF LDO

An FVF LDO with an on-chip output capacitor is implemented in [6], as shown in Fig. 2.13. The authors in [6] mention that it is difficult for the STC LDO topology to be stable with output dominant pole for a large on-chip capacitor (100 pF – 1 nF). Therefore, the proposed design in [6] employs the technique of buffer impedance attenuation to be stable with an output dominant pole. This design has a triple input error amplifier which helps improving the load regulation. This circuit also solves the problem of minimum load current requirement.

In [10] a simple voltage follower drives the pass transistor, whereas in this design a folded flipped voltage follower (FFVF) is used. As discussed earlier, using a voltage follower to drive the pass transistor decreases the impedance associated with the pass gate, moving that pole to high frequency. According to [11], the FFVF has much lower output impedance than the simple voltage follower. Therefore using the FFVF instead of a simple voltage follower can push the pole to a much higher frequency. In Fig. 2.13 transistors $M_9-M_{13}$ forms the FFVF. Placing this buffer in the feedback loop of the FVF avoids node $V_A$ from directly driving the gate of $M_{PASS}$, reducing the capacitance associated with node $V_A$. So, this
also moves the pole at node $V_A$ to a higher frequency. Therefore, the circuit in Fig. 2.13 circuit moves the internal poles to high frequencies to make the output pole dominant.

Similar to the STC LDO in [2], $V_{REF}$ and $V_{MIR}$ are the inputs to the error amplifier. But, in addition to them, there is another input which is $V_{OUT}$. So unlike the designs in [2], in [10] the output voltage is fed back to the error amplifier. The EA compares both $V_{MIR}$ and $V_{OUT}$ to $V_{REF}$ to generate the error signal. This also creates another negative feedback loop to regulate the output voltage apart from the conventional local loop of the FVF. According to [6], this improves the DC accuracy. However, the output voltage is still the mirrored from $V_{MIR}$.

Despite the use of a triple-input error amplifier, the loop gain for the regulating loop in [6] is low, resulting in deficient load regulation. Our proposed design enhances the load regulation by introducing another loop. While the LDO in [6] has a single compensation capacitor $CB$, another compensation network is introduced in the proposed design to make the LDO stable. This also results in reducing the disturbance on $V_{OUT}$ during a load transient.
Chapter 3

DESIGN AND SIMULATION RESULTS

This chapter describes the scaling of a fully integrated FVF LDO, the proposed FVF LDO design and its operation. Simulation results of the proposed design are also discussed in this chapter.

3.1 Scaling Fully Integrated FVF LDO from 65-nm to 180-nm process

The proposed multi-loop LDO is an enhanced version of the work presented in [6]. The LDO in [6] was implemented in a 65-nm CMOS process. However, in this work we selected a low-cost 180-nm process. In order to scale the design to a different process node, a scaling factor of the ratio of the maximum supply voltage of 180 nm core devices to those of 65-nm core devices is chosen. Therefore, scaling factor is

\[
\frac{1.8}{1.2} = 1.5
\]

Therefore, scaling factor is

Table 3.1 shows the scaled specifications.

3.2 Proposed Multi-loop FVF LDO

Fig. 3.1 shows the architecture of the proposed multi-loop LDO. Loop1 consists of a Folded Flipped Voltage Follower (FFVF) driving an output FVF stage. Loop1 by itself can regulate the output voltage but exhibits poor load regulation owing to its low loop gain. The low output impedance of the FVF

21
<table>
<thead>
<tr>
<th></th>
<th>[6]</th>
<th>Proposed Design</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage (V)</td>
<td>1.2</td>
<td>1.8</td>
</tr>
<tr>
<td>Output Voltage (V)</td>
<td>1</td>
<td>1.5</td>
</tr>
<tr>
<td>Dropout Voltage (mV)</td>
<td>150</td>
<td>225</td>
</tr>
<tr>
<td>$I_Q$ (low load-full load) ($\mu$A)</td>
<td>50 - 90</td>
<td>50 - 90</td>
</tr>
<tr>
<td>Load Current (mA)</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>Load Regulation (mV/mA)</td>
<td>1.1</td>
<td>0.11</td>
</tr>
</tbody>
</table>

Table 3.1: Scaled specifications.

stage provides a high unity gain frequency (UGF) for Loop1 [1]. This enables it to react immediately to changes in the load current. Loop2 consists of an error amplifier (EA1) and is predominantly used to set a left-half-plane (LHP) zero which aids in the stabilization of the LDO. Another function of Loop2 is the generation of voltage $V_{SET}$. The authors in [6] claim that sufficient DC accuracy of the LDO is achieved through the introduction of Loop3. Loop3 enhances the DC accuracy through the connection of $V_{OUT}$ to one input of the error amplifier (EA1).

The proposed work introduces a second error amplifier (EA2) in Loop4 to greatly enhance the load regulation.

Fig. 3.2 depicts the schematic of the proposed LDO. Transistors $M_1$-$M_5$ constitute the triple-input NMOS differential amplifier. Feedback from $V_{MIR}$ to transistor $M_2$ forms Loop2, as described above. The output of EA2, $V_B$, drives transistor $M_1$. Transistor $M_3$ forms the third input for the error amplifier, allowing feedback from $V_{OUT}$, thereby enhancing DC accuracy. The output of EA1 is $V_{EA}$; $V_{EA}$ is amplified further by PMOS common source amplifier $M_6$, to generate $V_{MIR}$. Control voltage $V_{SET}$, required for the output FVF stage, is generated using
Figure 3.1: Block diagram of proposed multi-loop FVF LDO.

transistors $M_6$, $M_7$ and $M_{15}$. $V_{SET}$ is generated through the diode-connection of transistor $M_7$ and is used to bias $M_8$ in the output FVF stage. A compensation capacitor $C_B$ is required to ensure stability of the FVF LDO [6]. The buffered FVF technique is implemented using an FFVF due to its extremely low output impedance compared to a regular voltage buffer [6], [11].

Figure 3.2: Architecture of proposed multi-loop FVF LDO.

An FFVF buffer is constructed using transistors $M_9 - M_{13}$. As described in section [2,5] introducing an FFVF moves the poles at both $V_G$ and $V_A$ away from
the output dominant pole. Transistor $M_9$ also acts as a level-shifter to remove the minimum load current requirement, as explained in section 2.4.2.

The schematic of EA2 is shown in the Fig. 3.3. It is a two-input differential amplifier, with an input bias current of 1 $\mu$A and a total quiescent current of 3 $\mu$A. Transistors $M_1$ and $M_2$ form the input pair, $M_3$ and $M_4$ constitute the conventional PMOS current mirror load, whereas $M_5$ is the tail transistor. Device sizes of EA2 are shown in the Table. 3.2

![Schematic of error amplifier](image)

Figure 3.3: Schematic of error amplifier2.

<table>
<thead>
<tr>
<th>Device</th>
<th>Sizing [$\mu$m/nm]</th>
</tr>
</thead>
<tbody>
<tr>
<td>$M_1$, $M_2$</td>
<td>$\frac{5}{540}$, m=1</td>
</tr>
<tr>
<td>$M_3$, $M_4$</td>
<td>$\frac{10}{540}$, m=1</td>
</tr>
<tr>
<td>$M_5$</td>
<td>$\frac{2.5}{540}$, m=2</td>
</tr>
<tr>
<td>$M_6$</td>
<td>$\frac{2.5}{540}$, m=1</td>
</tr>
</tbody>
</table>

Table 3.2: Device Sizes of EA2
The input bias current of the LDO is 903 nA. The quiescent current in the folded branch of the FFVF varies from 0 µA to 40 µA when switching from no load to full load respectively. Therefore, the overall quiescent current of the LDO varies from 53 µA to 93 µA. The sizes of transistors and values of compensation elements are shown in the Table.

3.2.1 Operation

Input transistors of $E_{A1}$, $M_2$ and $M_3$ are sized $\frac{3}{4}$th and $\frac{1}{4}$th of the size of $M_1$, respectively. This sizing explains the relationship between $V_B$ and $V_{OUT}$.

It is given by

\begin{equation}
\left( V_B - \frac{1}{4} \cdot V_{MIR} - \frac{3}{4} \cdot V_{OUT} \right) \cdot A_{EA} = V_{OUT} \tag{3.2}
\end{equation}

\begin{equation}
V_{MIR} = V_{OUT} + \Delta V \tag{3.3}
\end{equation}

where $A_{EA}$ is the gain from $EA1$ and the $V_{SET}$ generation stage and $\Delta V$ is the systematic and random mismatch between $V_{MIR}$ and $V_{OUT}$.

From (3.2) and (3.3) and $A_{EA}$ is very high, we find that

\begin{equation}
V_{OUT} = V_B - \Delta V/4 \tag{3.4}
\end{equation}

This states that $V_{OUT}$ is held closer to $V_B$ than to $V_{MIR}$. Now $V_B$ acts as the internal reference to the LDO.

To illustrate the function of Loop3, let us consider the case when $V_{OUT}$ increases beyond the desired voltage. When $V_{OUT}$ increases, the gate voltage of $M_3$ increases which is the positive input terminal of error amplifier $EA1$. Therefore, the output of the error amplifier, node $V_{EA}$ increases. This decreases the overdrive.
<table>
<thead>
<tr>
<th>Device</th>
<th>Sizing [µm/nm]</th>
</tr>
</thead>
<tbody>
<tr>
<td>$M_1$</td>
<td>$\frac{1.5}{540}$, m=1</td>
</tr>
<tr>
<td>$M_2$</td>
<td>$\frac{1}{4} \cdot \frac{1.5}{540}$, m=1</td>
</tr>
<tr>
<td>$M_3$</td>
<td>$\frac{3}{4} \cdot \frac{1.5}{540}$, m=1</td>
</tr>
<tr>
<td>$M_4$, $M_5$</td>
<td>$\frac{1.5}{540}$, m=2</td>
</tr>
<tr>
<td>$M_6$</td>
<td>$\frac{1.5}{540}$, m=4</td>
</tr>
<tr>
<td>$M_{16}$</td>
<td>$\frac{1.5}{540}$, m=1</td>
</tr>
<tr>
<td>$M_{15}$</td>
<td>$\frac{1.5}{540 \text{ nm}}$, m=3</td>
</tr>
<tr>
<td>$M_{12}$</td>
<td>$\frac{1.5}{540 \text{ nm}}$, m=11</td>
</tr>
<tr>
<td>$M_{14}$</td>
<td>$\frac{1.5}{540 \text{ nm}}$, m=10</td>
</tr>
<tr>
<td>$M_{10}$</td>
<td>$0.293 \frac{1.5}{540}$, m=11</td>
</tr>
<tr>
<td>$M_{11}$</td>
<td>$\frac{32}{1080}$</td>
</tr>
<tr>
<td>$M_{19A}$, $M_{19B}$</td>
<td>$\frac{1.5}{1080}$, m=2</td>
</tr>
<tr>
<td>$M_{17A}$, $M_{17B}$, $M_{18A}$, $M_{18B}$</td>
<td>$\frac{1.5}{540}$</td>
</tr>
<tr>
<td>$M_7$, $M_9$</td>
<td>$\frac{1.5}{180}$, m=3</td>
</tr>
<tr>
<td>$M_8$</td>
<td>$\frac{1.5}{180}$, m=10</td>
</tr>
<tr>
<td>$M_{13}$</td>
<td>$\frac{1.5}{180}$, m=8</td>
</tr>
<tr>
<td>$M_{PASS}$</td>
<td>$\frac{7.4}{180}$, m=43</td>
</tr>
<tr>
<td>$C_B$</td>
<td>8 pF</td>
</tr>
<tr>
<td>$R_C$</td>
<td>2 kΩ</td>
</tr>
<tr>
<td>$C_C$</td>
<td>5 pF</td>
</tr>
<tr>
<td>$C_R$</td>
<td>10 pF</td>
</tr>
</tbody>
</table>

Table 3.3: Device Sizes of Proposed Design
voltage of transistor $M_6$, sourcing less current to node $V_{MIR}$. This results in the
decrease of potential at node $V_{MIR}$, as there is a constant current being pulled
down from node $V_{MIR}$ by transistor $M_{15}$. The decrease in the potential at node $V_{MIR}$ also reflects in the output node $V_{OUT}$ because of the current mirror formed
by $M_7$ and $M_8$. Thus $V_{OUT}$ is brought back to the desired value.

Conversely, when the output voltage goes low, as it is the positive input
terminal for error amplifier EA1, output voltage $V_{EA}$ also decreases. This increases
the source-to-gate voltage of $M_6$, sourcing more current onto node $V_{MIR}$. As a
result, the voltage at node $V_{MIR}$ goes up, which also reflects on $V_{OUT}$.

But the above explained regulation of the output voltage depends upon
the loop gain of Loop3. However, Loop2 forces EA1 to operate in the unity gain
configuration, killing the loop gain of Loop3.

To further enhance the DC accuracy, a second error amplifier (EA2) is
introduced, as shown in Fig. 3.2. The positive input terminal of EA2 is held at reference voltage $V_{REF}$. Node $V_{OUT}$ is fed back to the negative terminal of EA2
to form Loop4 through the connection of node $V_B$ to the gate of transistor $M_1$.

Loop4 regulates $V_{OUT}$ to be equal to $V_{REF}$, while error amplifier $EA2$
contributes to the loop gain. An integrating capacitor $C_R$ is required to stabilize
Loop4. To explain the function of Loop4, let us consider a case where the output
voltage increases. If $V_{OUT}$ increases, the negative input terminal of EA2 goes
high. Therefore, the voltage at the output node of EA2, $V_B$ goes low. $V_B$ being
the negative terminal of EA1, when $V_B$ decreases, output voltage $V_{EA}$ increases.
An increase in $V_{EA}$ decreases the overdrive voltage of $M_6$, yielding less current
to $V_{MIR}$. As a result the voltage at node $V_{MIR}$ decreases, reducing the output
voltage. Loop4 regulates the output voltage through the same negative feedback
loop even when the output voltage is decreased.
An FFVF driving an FVF forms Loop1. An FVF, which is known for its fast transient response, helps Loop1 to react quickly to changes in the output voltage. If the output voltage is increased, $M_8$ being a common-gate amplifier, amplifies the change in the output which increases the voltage at the gate of $M_9$. As a result, the overdrive voltage of $M_9$ is decreased, sourcing less current to node $V_D$. Decreasing the voltage at node $V_D$ reduces the gate-to-source voltage of $M_{13}$, increasing the voltage at node $V_G$. With the increase in voltage at $V_G$, the source-to-gate voltage of $M_{PASS}$ decreases, sourcing less current to the output node. Therefore output voltage is decreased. However, as mentioned earlier, the low loop gain of the FVF results in poor load regulation.

3.3 Simulation Results

This section contains AC and transient simulations of the proposed LDO.

3.3.1 AC analysis

AC small-signal analysis is performed on the proposed multi-loop LDO to verify its stability across the complete load range. In order to accurately deduce the magnitude and phase response of individual loops, the signal path of each loop is broken at a particular node, as shown in Fig. 3.4.

To explain the AC analysis of individual loops conveniently, let us name the gate nodes of transistors $M_1$, $M_2$, $M_3$ and $M_9$ as $V_{fb4}$, $V_{fb2}$, $V_{fb3}$ and $V_{fb1}$, respectively, as shown in Fig. 3.5.

When Loop1 is broken at node $V_A$, node $V_A$ loses the loading effect of the parasitic capacitance associated with the input transistor of the FFVF buffer [6]. To mimic the loading effect, a parasitic loading stage is added, as shown in Fig. 3.5 [2]. The transistors in the parasitic loading stage are sized identical.
to the actual transistors in the LDO, so that it mimics the loading effect. Transistors $M_{9R}$-$M_{13R}$ form the parasitic loading stage. The gates of $M_{11R}$ and $M_{11}$ are connected together to bias $M_{11R}$, and also the gates of $M_{12R}$ and $M_{12}$ are connected together to bias $M_{12R}$.

Another important point to note is the requirement to isolate the effects of other loops on Loop1. So, node $V_{SET}$ is also considered as a break point for

Figure 3.5: Replicating the Input Capacitance of the FFVF Buffer on node $V_A$. 
Loop1. As such, a DC voltage source is used to establish the operating conditions for transistor $M_8$.

A large resistor is used to break the loop in each AC analysis test bench. The test bench for the AC analysis of Loop1 is shown in Fig. 3.6 (The test bench does not show the parasitic loading stage). An AC signal of magnitude 1 and phase 180° is fed into node $V_{fb1}$, such that the phase plot starts from 0°. The output is observed at node $V_A$. The magnitude and phase response of Loop1 at full load and no load condition are shown in Fig. 3.7. Table 3.4 summarizes the results of AC analysis of Loop1. Loop1 contributes to the fast transient response of the LDO, with a very high UGF of 180.5 MHz at 10mA of load current.

![Figure 3.6: Test bench for AC analysis of Loop1.](image)

Fig. 3.8 shows the magnitude and phase response of Loop1, illustrating the requirement of compensation network. We note that without the compensation network $Z_C$, Loop1’s phase margin is 6°. With the introduction of compensation network at node $V_D$, as shown in Fig. 3.2, Loop1’s phase margin improves to 26°.

Fig. 3.9 shows the test bench for AC analysis of Loop2. Loops 3 and 4 are also broken to obtain the frequency response of Loop2. An AC signal of
Figure 3.7: Loop1 AC analysis.

<table>
<thead>
<tr>
<th>Load Current (mA)</th>
<th>10</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain Margin (dB)</td>
<td>5.19</td>
<td>15.36</td>
</tr>
<tr>
<td>Phase Margin (Degrees)</td>
<td>26</td>
<td>73.7</td>
</tr>
<tr>
<td>Loop Gain (dB)</td>
<td>26.5</td>
<td>35.6</td>
</tr>
<tr>
<td>UGF (MHz)</td>
<td>180.5</td>
<td>9.1</td>
</tr>
</tbody>
</table>

Table 3.4: Simulated Results of AC Analysis of Loop1.

Figure 3.8: Magnitude and phase response of Loop1 with and without compensation network $Z_C$. 
magnitude 1 and phase 180° is fed into node $V_{fb2}$. The output is observed at node $V_{MIR}$. Fig. 3.10 shows the magnitude and phase response of Loop2 at full load and no load. Results of AC analysis are summarized in the Table 3.5.

Figure 3.9: Test bench for AC analysis of Loop2.

<table>
<thead>
<tr>
<th>Load Current (mA)</th>
<th>10</th>
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</tr>
</thead>
<tbody>
<tr>
<td>Gain Margin (dB)</td>
<td>34</td>
<td>40.1</td>
</tr>
<tr>
<td>Phase Margin (Degrees)</td>
<td>82.2</td>
<td>88.4</td>
</tr>
<tr>
<td>Loop Gain (dB)</td>
<td>51.9</td>
<td>48.5</td>
</tr>
<tr>
<td>UGF (MHz)</td>
<td>31.4</td>
<td>20.26</td>
</tr>
</tbody>
</table>

Table 3.5: Simulated results for AC analysis of Loop2.

Frequency plots of Loop3 are obtained by breaking Loop3 at node $V_{OUT}$ and Loop4 at node $V_{B}$. Fig. 3.11 shows the test bench for the AC analysis of Loop3. An AC signal of magnitude 1 and phase 180° is fed into node $V_{fb3}$. the output is observed at node $V_{OUT}$. The magnitude and phase plots of Loop3 are
shown in the Fig. 3.12. As Loop2 kills the gain of Loop3, Table 3.6 shows that the loop gain is very low.

Figure 3.10: Loop2 AC Analysis.

Fig. 3.13 shows the test bench for AC analysis of Loop4. An AC signal of magnitude 1 and phase 180° is fed into node $V_{fb4}$. The output is observed at node $V_B$. The magnitude and phase response of Loop4 are shown in the Fig. 3.14.
Figure 3.12: Loop3 AC analysis.

<table>
<thead>
<tr>
<th>Load Current (mA)</th>
<th>10</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain Margin (dB)</td>
<td>27.2</td>
<td>8.5</td>
</tr>
<tr>
<td>Phase Margin (Degrees)</td>
<td>148.1</td>
<td>77.8</td>
</tr>
<tr>
<td>Loop Gain (dB).</td>
<td>1.2</td>
<td>7.51</td>
</tr>
<tr>
<td>UGF (MHz)</td>
<td>1.24</td>
<td>4.8</td>
</tr>
</tbody>
</table>

Table 3.6: Simulated results for AC analysis of Loop3.

From the Table 3.7 though Loop4 is the slowest loop with a UGF of 383.2 kHz. The moderate loop gain of 32dB is introduced to regulate the output voltage.

Figure 3.13: Test bench for AC analysis of Loop4.
Figure 3.14: Loop4 AC analysis.

<table>
<thead>
<tr>
<th></th>
<th>No Load</th>
<th>Full Load</th>
</tr>
</thead>
<tbody>
<tr>
<td>Load Current (mA)</td>
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<td>0</td>
</tr>
<tr>
<td>Gain Margin (dB)</td>
<td>36.2</td>
<td>22.6</td>
</tr>
<tr>
<td>Phase Margin (Degrees)</td>
<td>86.3</td>
<td>87.2</td>
</tr>
<tr>
<td>Loop Gain (dB)</td>
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<td>32.1</td>
</tr>
<tr>
<td>UGF (kHz)</td>
<td>383</td>
<td>393</td>
</tr>
</tbody>
</table>

Table 3.7: Simulated Results for AC Analysis of Loop4.

3.3.2 Line Transient

The implemented LDOs transient performance is characterized through line and load transient simulations. Fig. 3.15 depicts the test bench for line transient. A line transient step from 1.8V to 2V is applied at the input node $V_{DD}$ with a rise and fall time of 10 ns. Load current, $I_L$ was kept constant at 10 mA during this test. The response to the line transient is observed is at the output node $V_{OUT}$, as shown in Fig. 3.16. Table 3.8 summarizes the results of line transient.
3.3.3 Load Transient

Fig. 3.17 displays the test bench for load transient. A load transient step from 0 μA to 10 mA with rise and fall times of 10 ns is achieved at output node $V_{OUT}$ by toggling an output switch. An NMOS FET is used as the switch which is
Load Current (mA) & 1 \\
Overshoot (mV) & 44.4 \\
Undershoot (mV) & 44.2 \\
$\Delta V_{\text{OUT,SS}}$ (mV) & 4.8 \\
$\Delta V_{\text{OUT}}$ (mV) & 93.2 \\
t_{RH} (ns) & 11.1 \\
t_{RL} (ns) & 7.0 \\
Line Regulation (mV/V) & 24 \\

Table 3.8: Simulated Results of Line Transient.

designed to be capable of allowing 10 mA of current through it. When the switch is ON, the maximum load current of 10 mA is drawn from the output; when the switch is OFF, the load current is zero. The response for the load transient is observed at the output node $V_{\text{OUT}}$ and is shown in Fig. 3.18. Table 3.9 summarizes the results of load transient.

![Load transient test bench](image)

Figure 3.17: Load transient test bench.
3.3.4 Dropout Voltage

Fig. 3.19 shows the test bench employed to measure dropout voltage. A triangle wave varying from 0 V to 2 V with a time period of 1 s is applied at the input node $V_{DD}$. The load resistance, $R_L$, is held constant during the test. $R_L$ is selected such that $I_L = 10$ mA when $V_{OUT} = 1.5$ V. The response for the dropout 

\[ \Delta V_{OUT,SS} (mV) = 0.31 \]

\[ \Delta V_{OUT} (mV) = 96.1 \]

\[ t_{RH} (\text{ns}) = 85.9 \]

\[ t_{RL} (\text{ns}) = 6.73 \]

Load Regulation (mV/mA) 0.031
test is observed at the output node $V_{OUT}$ and is shown in Fig. 3.20. From the simulated response, the dropout voltage is computed as 225 mV.

![Diagram of dropout test bench](image)

**Figure 3.19: Dropout test bench.**

![Graph showing simulated response for dropout test](image)

**Figure 3.20: Simulated response for dropout test.**
Chapter 4

MEASURED RESULTS OF FULLY-INTEGRATED FVF LDOs

We have done chip level testing of two different LDO designs. Both the LDOs are designed to generate an output voltage of 1.5 V with an input voltage of 1.8 V at a maximum load current of 10 mA. Figs. 4.1 and Fig. 4.2 show the schematics of the reference design and feed-forward design, respectively. The feed-forward design is an improved version of the reference design through the introduction of a feed-forward path highlighted in red in Fig. 4.2.

![Figure 4.1: Schematic of reference design.](image)

4.1 Layout

The complete layout of a chip having the above two designs is shown in Fig. 4.3. The feed-forward design is laid out on left side of the chip. The output
capacitor of 130 pF is also integrated. The right side of the chip has the reference design, along with its output capacitor of 130 pF. For testing purposes, there are also two additional 130 pF capacitors (capacitor1 and capacitor 2), which are laid out close to the actual output capacitors. As such, measuring these capacitors will give an approximated value of the actual output capacitors after fabrication. The rest of the chip is filled with substrate contacts and metal layers in order to satisfy density requirement.

There are a set of power lines, \( V_{DD} \) and \( V_{SS} \), for the reference design and another set of \( V_{DD} \) and \( V_{SS} \) for the feed-forward design. There is also another \( V_{DD} \) for the pad ring. The supply and output wires are laid out with extra width as they carry the maximum current.

The layout of feed-forward design is shown in Fig. 4.4. The area of this LDO is 223.9 \( \mu m \times 353.8 \mu m \)

The layout of the reference design is shown in Fig. 4.5. The area of this LDO is 241.7 \( \mu m \times 384.9 \mu m \)
4.2 Test Apparatus

We used a Keithley 2230-30-1 DC power supply to generate 1.8 V and 0 V to test the chip. A Rigol DG4102 function generator is used to generate the pulse signal needed in load and line transient tests. A Tektronix MSO 3034 oscilloscope is used to observe the waveforms of transient analysis.
Figure 4.4: Layout of feed-forward design.

Figure 4.5: Layout of reference design.
4.3 Hardware Results

4.3.1 DC Accuracy of the LDOs

When the LDOs are tested for DC functionality, it is observed that, instead of regulating the output voltage at 1.5 V, both the designs show a decrease in output voltage with an increase in load current. Although LDOs are designed for maximum load current of 10 mA, it is observed that the feed-forward design generates an output voltage of 1.38 V at 1 mA and an even lower output voltage of 1.0 V at 7 mA. On the other hand, the reference design generates an output voltage of 1.17 V at load of 1 mA and 0.42 V at 7.6 mA.

Transient performance of both the designs are characterized through load and line transient tests at load currents of 1 mA. Dropout test is also performed to find out the dropout voltage, even though the output voltage is not the correct value.

4.3.2 Dropout

Input voltage is varied slowly from 0 V to 2 V to perform the dropout test. Fig. 4.6 and Fig. 4.7 shows the measured and simulated response of the feed-forward design respectively. The measured response of the reference design is shown in Fig. 4.8 and Fig. 4.9 shows the simulated response of the reference design.

Results from the hardware indicate that the reference design and feed-forward design are able to regulate the output voltage at 1.18 V and 1.38 V, respectively. Therefore, the output voltage of both the designs is lower than the desired output voltage of 1.5 V. A possible cause for this is low loop gain which happens when some of the transistors in the LDO operate in the linear region instead of saturation.
Figure 4.6: Measured dropout response of feed-forward design at $I_L = 1 \text{ mA}$.

<table>
<thead>
<tr>
<th>Design</th>
<th>Simulated dropout voltage</th>
<th>Measured dropout voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Feed-forward Design</td>
<td>58.6 mV</td>
<td>184 mV</td>
</tr>
<tr>
<td>Reference Design</td>
<td>98 mV</td>
<td>297 mV</td>
</tr>
</tbody>
</table>

Table 4.1: Comparison of dropout voltage at $I_L = 1 \text{ mA}$.

A comparison of measured and simulated dropout voltages at 1 mA load current is done in Table 4.1. It can be observed that measured the dropout voltage of both the designs are higher than the simulated values. This relates to the DC offset associated with output voltage i.e, the higher dropout voltage forces the output voltage to be less than the desired value.

4.3.3 Load Transient

A BJT is used as a load transient switch to toggle the load current from 10 mA to 0 mA. This is achieved by feeding a pulse waveform switching between
Figure 4.7: Simulated dropout response of feed-forward design at $I_L = 1$ mA.

0.75 V to 0 V into the base of the BJT. The BJT is turned ON for the input voltage level of 0.75 V, pulling a load current of 1 mA and it draws no current when it is turned OFF at 0 V. Rise and fall times of the pulse signal are adjusted such that load current is switched with rise and fall times of 10 ns. However, due to parasitics, actual rise and fall times of load current are significantly more than 10 ns as shown in the measured results from the oscilloscope.

Fig. 4.10 shows the measured response of the feed-forward design, whereas Fig. 4.11 shows the simulated response. Fig. 4.10 shows output and input waveforms on the top and bottom, respectively. In the measured result, the output voltage switches between a high level of 1.46 V and low level of 1.38 V, without
Figure 4.8: Measured dropout response of reference design at $I_L = 1$ mA.

exhibiting any undershoot and overshoot. Fig. 4.12 shows the output waveform, input waveform and the voltage at the collector of BJT, in that order, from top to bottom. Rise time and fall times of the load current are found by measuring the rise time and fall time of collector-voltage waveform, which are 195 ns and 79.4 ns respectively.

The load transient response of the reference design is shown in Fig. 4.13, whereas Fig. 4.14 shows the simulated response. In Fig. 4.13 the output waveform is the top trace and the input waveform is the bottom trace. From the measured result, it can be observed that the output voltage switches between a high level of 1.30 V and low level of 1.10 V without exhibiting undershoot or overshoot. Fig. 4.15 shows multiple cycles of the output waveform, the voltage at the collector of BJT and the input waveform, in that order, from top to bottom. The measured values of rise and fall times are 134 ns and 91.5 ns, respectively.
Figure 4.9: Simulated dropout response of reference design.

Table 4.2 summarizes the results of load transient for both the designs. Simulation results show that, a load transient of 1 mA with slow rise and fall times could not move the output voltage out of the 2 percent tolerance band. Therefore, recovery times of simulation results are not presented in the summary Table. 4.2

Large rise and fall times of load current helps the LDO to change voltage levels without having overshoot or undershoot. With no overshoot or undershoot, we were unable to measure the recovery times for load transient of both the designs. The output voltage signal also has an undesirable spike when it is changing from one level to another. This is because the input signal feed through from base-
<table>
<thead>
<tr>
<th></th>
<th>Feed-forward Design</th>
<th>Reference Design</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Simulated</td>
<td>Measured</td>
</tr>
<tr>
<td>Overshoot</td>
<td>12.6 mV</td>
<td>-</td>
</tr>
<tr>
<td>Undershoot</td>
<td>26.9 mV</td>
<td>-</td>
</tr>
<tr>
<td>$\Delta V_{\text{OUT,SS}}$</td>
<td>2.9 mV</td>
<td>75.4 mV</td>
</tr>
</tbody>
</table>

Table 4.2: Comparison of load transient parameters.

to-collector of the BJT via the input capacitance, causing spikes on the collector, which are replicated on the output voltage.

![Figure 4.10](image)  
Figure 4.10: Measured load transient response of feed-forward design.

### 4.3.4 Line Transient

The line transient test is performed by changing the supply voltage from 1.8 V to 2 V. This is achieved by feeding a pulse waveform of 250 kHz frequency into the input node. Rise and fall times of pulse signals are set to 10 ns. However,
Figure 4.11: Simulated load transient response of feed-forward design.

Figure 4.12: Measured load transient response of feed-forward design - multiple cycles.
Figure 4.13: Measured load transient response of reference design.

Figure 4.14: Simulated load transient response of reference design.
Figure 4.15: Measured load transient response of reference design - multiple cycles. Due to parasitics, actual rise and fall times are not 10 ns and are as shown in the measured results from oscilloscope. Fig. 4.16 shows the measured response of feed-forward design, whereas Fig. 4.17 shows the simulated response. From the measured result it can be observed that output voltage has steady-state values of 1.43 V and 1.36 V, respectively.

The measured response for line transient of reference design is shown in the Fig. 4.20 and Fig. 4.19 shows the simulated response. From the measured result it can be observed that output voltage has steady-state values of 1.23 V and 1.15 V after overshoot and undershoot, respectively. Recovery times after the undershoot and overshoot are measured using cursors on the oscilloscope and are shown in the Table 4.3. Figs. 4.18 and 4.21 show multiple cycles of measured line transient response for the feed-forward design and reference design, respectively.
Figure 4.16: Measured line transient response of feed-forward design.

Figure 4.17: Simulated line transient response of feed-forward design.
Table 4.3 summarizes the simulated and hardware results of line transient. It can be observed that the measured overshoot and undershoot are less than the simulated values. This is because the rise and fall times achieved in hardware are not as fast as those achieved in simulation. A possible cause for the measured recovery times to be higher than the simulated is undesired parasitics from hardware.

Fig. 4.22 shows the simulated load transient response of the feed-forward design and reference design. It can be observed that overshoot of the feed-forward design is almost 49% less than the reference design. However, we could not compare the overshoot in measured responses as they did not exhibit overshoot.

Figure 4.18: Measured line transient response of feed-forward design - multiple cycles.
Figure 4.19: Simulated line transient response of reference design.

Figure 4.20: Measured line transient response of reference design.
Figure 4.21: Measured line transient response of reference design - multiple cycles.

Table 4.3: Comparison of line transient parameters.

<table>
<thead>
<tr>
<th></th>
<th>Feed-forward Design</th>
<th>Reference Design</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Simulated</td>
<td>Measured</td>
</tr>
<tr>
<td>Overshoot</td>
<td>44.8 mV</td>
<td>39 mV</td>
</tr>
<tr>
<td>Undershoot</td>
<td>54.6 mV</td>
<td>33.3 mV</td>
</tr>
<tr>
<td>$t_{RH}$</td>
<td>191 ns</td>
<td>324 ns</td>
</tr>
<tr>
<td>$t_{RL}$</td>
<td>6.2 ns</td>
<td>76 ns</td>
</tr>
<tr>
<td>$\Delta V_{OUT,SS}$</td>
<td>3.23 mV</td>
<td>2.5 mV</td>
</tr>
</tbody>
</table>
Figure 4.22: Simulated load transient response of reference and simulated design.
Chapter 5

DISCUSSION AND CONCLUSION

A multi-loop FVF LDO is proposed with improved load regulation. A DC regulation loop (Loop4) is introduced to improve steady state output regulation of the FVF LDO. In simulation, the proposed LDO achieves a transient response time \( T_R \) of 0.73 ns while exhibiting an improved DC load regulation of 0.031 mV/mA. A \( \Delta V_{OUT} \) of 48 mV is measured through load transient simulation.

To compare this work with other LDOs in the literature, a widely-used response time \( T_R \) and figure-of-merit (FOM) are adopted from [12]. \( T_R \) is defined as

\[
T_R \equiv \frac{C \cdot \Delta V_{OUT}}{I_{MAX}} \quad (5.1)
\]

where \( \Delta V_{OUT} \) is the maximum variation in output voltage during the load transient and \( C \) is the total on-chip capacitance. The FOM is given by

\[
FOM \equiv T_R \cdot \frac{I_Q}{I_{MAX}} \quad (5.2)
\]

Therefore, FOM is a function of \( T_R \), total quiescent current \( I_Q \) and maximum load current \( I_{MAX} \). This indicates that, the lower the FOM, the better is the performance of the LDO.

From Table 5.1 it can be observed that the proposed LDO with the newly introduced Loop4 for improving DC accuracy also aids in enhancing the transient response time and thereby achieving an ultra low FOM of 3.9 ps. In comparison
with other work in the literature, as showcased in Table 5.1, the proposed LDO performs comparably in terms of dropout voltage, quiescent current consumption, transient response time, and DC load regulation.

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_L$</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Technology</td>
<td>90-nm</td>
<td>45-nm SOI</td>
<td>0.35µm</td>
<td>65-nm</td>
<td>65-nm</td>
<td>28-nm</td>
<td>180-nm</td>
</tr>
<tr>
<td>Vout</td>
<td>0.9V</td>
<td>0.9 to 1.1V</td>
<td>1.2V</td>
<td>1V</td>
<td>1V</td>
<td>0.87V</td>
<td>1.5V</td>
</tr>
<tr>
<td>Dropout</td>
<td>300 mV</td>
<td>85 mV</td>
<td>660 mV</td>
<td>200 mV</td>
<td>150 mV</td>
<td>200 mV</td>
<td>225 mV*</td>
</tr>
<tr>
<td>$I_Q$</td>
<td>6 mA</td>
<td>12 mA</td>
<td>44 µA</td>
<td>23.7 µA</td>
<td>50 to 90 µA</td>
<td>100 µA</td>
<td>53 to 93 µA</td>
</tr>
<tr>
<td>$I_{max}$</td>
<td>100 mA</td>
<td>42 mA</td>
<td>12 mA</td>
<td>50 mA</td>
<td>10 mA</td>
<td>10 mA</td>
<td>10 mA</td>
</tr>
<tr>
<td>Total Cap.</td>
<td>600 pF</td>
<td>1.46 nF</td>
<td>100 pF</td>
<td>27 pF</td>
<td>140 pF</td>
<td>120 pF</td>
<td>153 pF</td>
</tr>
<tr>
<td>$\Delta V_{OUT@T_{EDGE}}$</td>
<td>90 mV@100 ps</td>
<td>N/A</td>
<td>105 mV@500 ns</td>
<td>40 mV@200 ns</td>
<td>82 mV@1000 ps</td>
<td>26 mV@30 ps</td>
<td>48 mV@10 ns</td>
</tr>
<tr>
<td>DC Line Reg.</td>
<td>882 mV/V**</td>
<td>27 mV/V**</td>
<td>0.28 mV/V</td>
<td>8.89 mV/V</td>
<td>37.1 mV/V</td>
<td>NA</td>
<td>24 mV/V**</td>
</tr>
<tr>
<td>DC Load Reg.</td>
<td>0.9 mV/mA</td>
<td>0.083 mV/mA</td>
<td>0.68 mV/mA</td>
<td>0.034 mV/mA</td>
<td>1.1 mV/mA</td>
<td>NA</td>
<td>0.031 mV/mA*</td>
</tr>
<tr>
<td>$T_m$</td>
<td>0.54 ns</td>
<td>0.309 ns*</td>
<td>N/A</td>
<td>N/A</td>
<td>1.15 ns</td>
<td>312 ps</td>
<td>0.73 ns*</td>
</tr>
<tr>
<td>FOM</td>
<td>32 ps</td>
<td>62.4 ps*</td>
<td>N/A</td>
<td>N/A</td>
<td>5.74 ps</td>
<td>3.12 ps</td>
<td>3.9 ps*</td>
</tr>
</tbody>
</table>

Table 5.1: Summary and comparison of simulated results with the state-of-the-art LDOs.

* Simulated Results. ** Estimated from figure.

5.0.1 Issues

1. This architecture will be difficult to implement in legacy processes, such as 0.5 µm, because of increased parasitics, which leads to additional low frequency poles.

2. The fabricated design exhibits poor DC accuracy.

3. We could not achieve rise time and fall times of 10 ns in hardware measurement during the load transient test, because of significant input capacitance in the load transient switch. This can be avoided by integrating load transient switch in the IC.
4. It is possible that the loop gain interact in such a way that they are highly sensitive to one another. Sensitivity analysis and/or Monte Carlo analysis may be required in order to demonstrate the viability of either the 3-loop or 4-loop architectures.

5.0.2 Future Work

1. Developing the small signal model to understand how parasitics affect the performance of the proposed architecture.

2. Proposed design illustrates the technique of enhancing the load regulation by adding another loop to the existing local loop of FVF; Other methods of enhancing the loop gain of the FVF can be explored.
REFERENCES
REFERENCES


APPENDIX
APPENDIX

Test Document
A.1 Pin Description

This work is fabricated on Quad Flat Package (QFP) using IBM 0.18 µm CMOS process. In this 44-pin package, every 11th pin is not used as the pad frame consists of only 40 pins. Detailed description of individual pin is described in Table 1.

A.2 Supply Voltages and Currents

\[ V_{DD,F} = V_{DD,R} = 1.8 \text{ V} \]
\[ V_{SS,F} = V_{SS,R} = 0 \text{ V} \]
\[ V_{DD,PAD} = 1.8 \text{ V} \]
\[ V_{REF,F} = V_{REF,R} = 1.5 \text{ V} \]
\[ I_{BIAS,F} = I_{BIAS,R} = 1 \mu\text{A} \]

A.3 Test Procedure

A PCB is designed to characterize the chip, Fig. 1 shows the schematic of PCB.

**Pad ring, Reference voltage and Bias current:**

**Procedure:**

1. Power-supply LDO IC4 provides an output voltage of 1.8 V to power up pad ring, to generate bias currents and also to generate reference voltages for both the designs.
2. Use DC power supply from the lab to feed the SMA connector U8 with DC voltage of 2 V, this powers up LDO IC4. In-order to generate output voltage of 1.8 V from the LDO IC4, feedback resistors RF3 and RF4 are selected as per the guide lines mentioned in the datasheet of the LDO. RF3 and RF4 are chosen accordingly and are 1.19 kΩ and 9.4 kΩ respectively. Resistor pot POT_{VDDBIAS} is adjusted to fine tune the output voltage to 1.8 V.
### Table 1: Pin Description of Fabricated Chip.

<table>
<thead>
<tr>
<th>Pin #</th>
<th>Name</th>
<th>Pad type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>V(_{DD,PAD})</td>
<td>Bare Pad</td>
<td>Power supply for the pad ring</td>
</tr>
<tr>
<td>2-5</td>
<td>V(_{SS,F})</td>
<td>High Current Protected</td>
<td>Ground for feed-forward design</td>
</tr>
<tr>
<td>6-9</td>
<td>V(_{OUT,F})</td>
<td>High Current Protected</td>
<td>Output for feed-forward design</td>
</tr>
<tr>
<td>10</td>
<td>NOC</td>
<td>High Current Protected</td>
<td>No Connection</td>
</tr>
<tr>
<td>11</td>
<td>NOC</td>
<td>High Current Protected</td>
<td>No Connection</td>
</tr>
<tr>
<td>12</td>
<td>I(_{BIAS,F})</td>
<td>High Current Protected</td>
<td>Bias current for feed-forward design</td>
</tr>
<tr>
<td>13</td>
<td>V(_{REF,F})</td>
<td>High Current Protected</td>
<td>Reference voltage for feed-forward design</td>
</tr>
<tr>
<td>14</td>
<td>NOC</td>
<td>High Current Protected</td>
<td>No Connection</td>
</tr>
<tr>
<td>15</td>
<td>Capacitor1-terminal</td>
<td>High Current Protected</td>
<td>One terminal of capacitor1 where the other terminal is connected to ground of feed-forward design</td>
</tr>
<tr>
<td>16</td>
<td>NOC</td>
<td>High Current Protected</td>
<td>No Connection</td>
</tr>
<tr>
<td>17 - 21</td>
<td>V(_{DD,R})</td>
<td>High Current Protected</td>
<td>Power supply for reference design</td>
</tr>
<tr>
<td>22</td>
<td>NOC</td>
<td>High Current Protected</td>
<td>No Connect pin</td>
</tr>
<tr>
<td>23 - 26</td>
<td>V(_{SS,R})</td>
<td>High Current Protected</td>
<td>Ground for reference design</td>
</tr>
<tr>
<td>27 - 30</td>
<td>V(_{OUT,R})</td>
<td>High Current Protected</td>
<td>Output for reference design</td>
</tr>
<tr>
<td>31</td>
<td>V(_{REF,R})</td>
<td>High Current Protected</td>
<td>Reference voltage for reference design</td>
</tr>
<tr>
<td>32</td>
<td>NOC</td>
<td>High Current Protected</td>
<td>No Connection</td>
</tr>
<tr>
<td>33</td>
<td>NOC</td>
<td>High Current Protected</td>
<td>No Connection</td>
</tr>
<tr>
<td>34</td>
<td>I(_{BIAS,R})</td>
<td>High Current Protected</td>
<td>Bias current for reference design</td>
</tr>
<tr>
<td>35, 36</td>
<td>NOC</td>
<td>High Current Protected</td>
<td>No Connection</td>
</tr>
<tr>
<td>37</td>
<td>Capacitor2-terminal</td>
<td>High Current Protected</td>
<td>One terminal of capacitor2 where the other terminal is connected to ground of feed-forward design</td>
</tr>
<tr>
<td>38-42</td>
<td>V(_{DD,F})</td>
<td>High Current Protected</td>
<td>Power supply for feed-forward design</td>
</tr>
<tr>
<td>43, 44</td>
<td>NOC</td>
<td>High Current Protected</td>
<td>No Connection</td>
</tr>
</tbody>
</table>
3. Output voltage of LDO IC4 is connected to $V_{DD,\text{PAD}}$ (pin 1) to power up the pad ring.

4. Resistor divider formed by $R_{\text{VREF1}}$, $R_{\text{VREF2}}$ and the resistor pot R2 generates the reference voltage of 1.5 V from the output of LDO IC4. $R_{\text{VREF1}}$ and $R_{\text{VREF2}}$ are chosen accordingly and are 500 Ω and 4.23 kΩ respectively. Reference voltage is shared to pins $V_{\text{REF,F}}$, $V_{\text{REF,R}}$ (pins 31, 13).

5. Bias currents for both the designs are generated from the output of LDO IC4.
6. The value of bias resistor \( R_{BIAS} \) to generate 1 µA of bias current from the output of LDO IC4 is calculated from the equation:

\[
V_{GS,NMOS} = 0.5 \, V \\
V_{OUT} = 1.8 \, V \\
I_{BIAS} = 1 \, \mu A \\
R_{BIAS} = \frac{V_{OUT} - (V_{GS,NMOS})}{I_{BIAS}} \tag{1}
\]

From the above equations, we get

\[ R_{BIAS} = 1.3 \, M\Omega \]

7. Parallel combination of resistors \( R_{IB1} \) and \( R_{IB2} \) forms the bias resistor for reference design and the parallel combination of resistors \( R_{IBR1} \) and \( R_{IBR2} \) forms the bias resistor for feed-forward design.

8. Therefore \( R_{IB1} = 2.71 \, M\Omega \), \( R_{IB2} = 2.5 \, M\Omega \), \( R_{IBR1} = 2.71 \, M\Omega \) and \( R_{IBR2} = 2.5 \, M\Omega \).

**Dropout Test for Reference Design:**

**Procedure:**

1. Close the path-2 in jumper JP1 and path-1 in jumper JP\(_{OUT1}\).

2. Value of load resistor to draw 1 mA of load current is calculated from the equation below:

\[
V_{OUT} = 1.18 \, V \\
I_{Load} = 1 \, mA \\
R_{Load} = \frac{V_{OUT}}{I_{Load}} \tag{2}
\]

70
3. From the above equations, $R_{Load} = 1.18 \, k\Omega$.

4. Parallel combination of RL9 and RL10 forms the load resistor $R_{Load}$.

5. Therefore $RL9 = RL10 = 2.32k\Omega$.

6. Generate the necessary bias current and reference voltage as described in the procedure for reference voltage and bias current.

7. Set up the waveform generator to source a slow triangle signal varying from 0 to 2 V with a time period of 1 second.

8. Feed SMA connector U3 with the signal from the waveform generator.

9. Probe the output node at either of RL10 and RL9 to observe the output response on the oscilloscope screen.

**Dropout Test for Feed-forward Design:**

**Procedure:**


2. Value of load resistor to draw 1 mA of load current is calculated from the equation below:

   \[
   V_{OUT} = 1.38 \, V \\
   I_{Load} = 1 \, mA \\
   R_{Load} = \frac{V_{OUT}}{I_{Load}}
   \]  

   (3)

3. From the above equations, $R_{Load} = 1.38 \, k\Omega$.

4. Parallel combination of RL1 and RL2 forms the load resistor $R_{Load}$.

5. Therefore $RL1 = 2.8 \, k\Omega$ and $RL2 = 2.66 \, k\Omega$.

6. Generate the necessary bias current and reference voltage as described in the procedure for reference voltage and bias current.
7. Set up the waveform generator to source a slow triangle signal varying from 0 to 2 V with a time period of 1 second.

8. Feed SMA connector U2 with the signal from the waveform generator.

9. Probe the output node at either RL1 or RL2 to observe the output response on the oscilloscope screen.

Load Transient for Reference Design:

Procedure:

1. Setup the waveform generator to source a pulse signal switching between 0.75 V to 0 V with a frequency of 250 kHz. Adjust the rise and fall times to 10 ns.

2. Parallel combination of resistors RL11 and RL12 forms the load resistor $R_{\text{Load}}$, parallel combination of resistors RL13 and RL14 forms the base-resistor whereas the emitter-resistor is formed by the parallel combination of RL15 and RL16.

3. Choose emitter-resistor and base-resistor of BJT T1 such that both base-emitter and base-collector junctions are forward biased when the input signal is 0.75 V. Base-resistor and emitter-resistor are chosen accordingly and are 60 Ω and 45 Ω respectively.

4. Value of load resistor to draw 1 mA of load current is calculated from the equation below:

\[
R_{\text{Load}} = \frac{V_{\text{OUT}} - (V_{\text{Collector}})}{I_{\text{Load}}} \quad (4)
\]
From the above equations, we get

\[ R_{\text{Load}} = 400 \, \Omega \]

5. Therefore, \( RL11 = RL12 = 800 \, \Omega \).

6. Close path-3 in jumper JP1 and path-2 in jumper JP_{OUT1}.

7. Generate the bias current and reference voltage as described in the procedure for reference voltage and bias current.

8. Feed the SMA connector U7 with a DC voltage of 2 V, this powers up LDO IC3. In-order to generate output voltage of 1.8 V from the LDO IC3, feedback resistors RF1 and RF2 are selected. as per the guide lines mentioned in the datasheet of the LDO and are 1.19 kΩ and 9.4 kΩ respectively. Resistor pot \( POT_{VDD} \) is adjusted to fine tune the output voltage to 1.8 V.

9. Feed the SMA connector U4 with the signal from the waveform generator.

10. Probe the output node at either RL11 or RL12 to observe the output signal on oscilloscope.

11. Probe the collector of BJT to measure the rise and fall times of load current.

**Load Transient for Feed-forward Design:**

**Procedure:**

1. Setup the waveform generator to source a pulse signal switching between 0.75 V to 0 V with a frequency of 250 kHz. Adjust the rise and fall times to 10 ns.

2. Parallel combination of resistors RL3 and RL4 forms the load resistor \( R_{\text{Load}} \), parallel combination of resistors RL5 and RL6 forms the base-resistor whereas the emitter-resistor is formed by the parallel combination of RL7 and RL8.
3. Choose emitter-resistor and base-resistor of BJT T2 such that both base-emitter and base-collector junctions are forward biased when the input signal is 0.75 V. Base-resistor and emitter-resistor are chosen accordingly and are 60 Ω and 45 Ω respectively.

4. Value of load resistor to draw 1 mA of load current is calculated from the equation below:

\[
V_{Collector} = 0.7 \, V \\
V_{OUT} = 1.39 \, V \\
I_{Load} = 1 \, mA \\
R_{Load} = \frac{V_{OUT} - (V_{Collector})}{I_{Load}} \\
\] (5)

From the above equations, we get

\[
R = 1.32 \, k\Omega
\]

5. Therefore RL3 = RL4 = 2.66 kΩ.

6. Close path-3 in jumper JP2 and path-1 in jumper JP_{OUT2}.

7. Generate the bias current and reference voltage as described in the procedure for reference voltage and bias current.

8. Use DC power supply from the lab to provide a DC voltage of 2 V to the SMA connector U9, this powers up LDO IC2. In-order to generate output voltage of 1.8 V from the LDO IC2, feedback resistors RF5 and RF6 are chosen as per the guide lines mentioned in the datasheet of the LDO and are 1.19 kΩ and 9.4 kΩ respectively. Resistor pot POT_{VDD2} is adjusted to fine tune the output voltage to 1.8 V.
9. Feed the SMA connector U1 with the signal from the waveform generator.

10. Probe the output node at either RL3 or RL4 to observe the output signal on oscilloscope.

11. Probe the collector of BJT T2 to measure the rise and fall times of load current.

Line Transient for Reference Design:

Procedure:

1. Close the path 2 in jumper JP1 and path 1 in jumper \( JP_{OUT1} \)

2. Choose the load resistor \( R_{Load} \) to draw 1 mA of current through the output

\[
V_{OUT} = 1.18 \, V \\
I_{Load} = 1 \, mA \\
R_{Load} = \frac{V_{OUT}}{I_{Load}} \tag{6}
\]

3. From the above equations, \( R_{Load} = 1.18 \, k\Omega \).

4. Parallel combination of RL9 and RL10 forms the load resistor \( R_{Load} \).

5. Therefore RL9 = RL10 = 2.32 k\Omega.

6. Generate the necessary bias current and reference voltage as described in the procedure for reference voltage and bias current.

7. Set up the waveform generator to source a pulse signal varying from 1.8 V to 2 V with a frequency of 250 kHz. Set the rise and fall time of pulse signal as 10 ns.

8. Feed SMA connector U3 with the signal from the waveform generator.
9. Probe the output node at either of RL10 and RL9 to observe the output response on the oscilloscope screen.

**Line Transient for Feed-forward Design:**

**Procedure:**

1. close the path-2 in jumper JP2 and path-2 in jumper $JP_{OUT2}$.

2. Choose the load resistor $R_{Load}$ to draw 1 mA of current through the output.

$$V_{OUT} = 1.38 \, \text{V}$$

$$I_{Load} = 1 \, \text{mA}$$

$$R_{Load} = \frac{V_{OUT}}{I_{Load}} \quad (7)$$

3. From the above equations, $R_{Load} = 1.38 \, \Omega$.

4. Parallel combination of RL1 and RL2 forms the load resistor $R_{Load}$.

5. Therefore $RL1 = 2.8 \, \text{k}\Omega$, $RL2 = 2.66 \, \text{k}\Omega$

6. Generate the necessary bias current and reference voltage as described in the procedure for reference voltage and bias current.

7. Set up the waveform generator to source a pulse signal varying from 1.8 V to 2 V with a frequency of 250 kHz. Set the rise and fall time of pulse signal as 10 ns.

8. Feed SMA connector U2 with the signal from the waveform generator.

9. Probe the output node at either RL1 or RL2 to observe the output response on the oscilloscope screen.