

# Wenjie Che

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## Education

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PhD in Computer Engineering, University of New Mexico 2016.12  
Master of Engineering, Computer Technology, Hunan University, China 2013.6  
Bachelor of Science, Telecommunications Engineering, Hunan Normal University, China 2010.6

## Professional Experience

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Klipsch School of Electrical and Computer Engineering, New Mexico State University  
Assistant Professor 2018.8 ~ present

Enthentica Inc.  
Research Scientist 2017.1 ~ 2018.4

## Research Interests

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- Hardware security and trust, cryptography primitives and authentication protocols
- Embedded systems, hardware software co-design
- Machine learning, model building attacks
- Design for test, automatic test pattern generation (ATPG)

## Publications

(Google scholar link: [https://scholar.google.com/citations?user=ItGTO\\_EAAAAJ&hl=en](https://scholar.google.com/citations?user=ItGTO_EAAAAJ&hl=en) )

### Journal Publications

- [J11] I Bow, N Bete, F Saqib, **W. Che**, C Patel, R Robucci, C Chan, J Plusquellic, "Side-Channel Power Resistance for Encryption Algorithms Using Implementation Diversity", *Cryptography*, vol. 4, no. 2, 2020.
- [J10] J Calhoun, C Minwalla, C Helmich, F Saqib, **W. Che**, J Plusquellic, "Physical Unclonable Function (PUF)-Based e-Cash Transaction Protocol (PUF-Cash)," *Cryptography*, vol. 3, no. 3, 2019.
- [J9] **W. Che**, F. Saqib, J. Plusquellic, "Novel Offset Techniques for Improving Bitstring Quality of a Hardware-Embedded Delay PUF," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 26, no. 4, pp. 733-743, April 2018.
- [J8] D. Owen Jr., D. Heeger, C. Chan, **W. Che**, F. Saqib, M. Areno and J. Plusquellic, "An Autonomous, Self-Authenticating and Self-Contained Secure Boot Process for FPGAs", *Cryptography (MDPI)*, vol. 2, no. 3, 2018
- [J7] **W. Che**, V. K. Kajuluri, F. Saqib, J. Plusquellic, "Leveraging Distributions in Physical Unclonable Functions," *Cryptography*, vol. 1, no. 3, 2017.
- [J6] **W. Che**, V. K. Kajuluri, M. Martin, F. Saqib, J. Plusquellic, "Analysis of Entropy in a Hardware-Embedded Delay PUF," *Cryptography*, vol. 1, no. 1, 2017.

- [J5] **W. Che**, M. Martin, G. Pocklassery, V. K. Kajuluri, F. Saqib, J. Plusquellic, "A Privacy-preserving, Mutual PUF-Based Authentication Protocol," *Cryptography*, vol. 1, no. 1, 2016.
- [J4] **W. Che**, Y. Lin, A. Pan, J. Zhang, "A Robust Hierarchical FSM Structure for Active IC Metering," *Information Technology Journal*, vol. 12, no. 6, pp. 1107-1115, 2013.
- [J3] A. Pan, Y. Lin, **W. Che**, Z. You, Y. Liu, J. Li, "A comprehensive metering scheme for intellectual property protection during both after-sale and evaluation periods of IC design," *IEICE Electronic Express*, vol. 10, no. 19, pp. 1-11, 2013.
- [J2] J Zhang, Y Lin, **W. Che**, Q Wu, Y Lu, K Zhao, "Efficient verification of IP watermarks in FPGA designs through lookup table content extracting," *IEICE Electronics Express*, vol. 9, no. 22, pp. 1735-1741, 2012.
- [J1] J Zhang, Y Lin, Q Wu, **W. Che**, "Watermarking FPGA Bitfile for Intellectual Property Protection," *Radioengineering*, vol. 21, no. 2, pp. 764-771, 2012.

### **Conference Publications**

- [C7] **W. Che**, M. Martinez-Ramon, F. Saqib, J. Plusquellic, "Delay Model and Machine Learning Exploration of a Hardware-Embedded Delay PUF," in *IEEE International Symposium on Hardware Oriented Security and Trust (HOST)*, 2018, pp. 153-158.
- [C6] G. Pocklassery, **W. Che**, F. Saqib, M. Areno and J. Plusquellic, "Self-Authenticating Secure Boot for FPGAs," in *IEEE International Symposium on Hardware Oriented Security and Trust (HOST)*, 2018, pp. 221-226.
- [C5] A. S. Siddiqui, C.-C. Lee, **W. Che**, J. Plusquellic and F. Saqib, "Secure Intra-Vehicular Communication over CANFD", *AsianHOST*, 2017, pp. 97-102.
- [C4] **W. Che**, F. Saqib, J. Plusquellic, "PUF-based authentication", *Proc. IEEE/ACM Int. Conf. Comput.-Aided Design (ICCAD)*, pp. 337-344, 2015.
- [C3] **W. Che**, J. Plusquellic, S. Bhunia, "A Non-volatile Memory Based Physically Unclonable Function without Helper Data", *ICCAD 2014*, pp. 148-153.
- [C2] J Zhang, Y Lin, Y Lyu, RCC Cheung, **W. Che**, Q Zhou, J Bian, "Binding hardware IPs to specific FPGA device via inter-twining the PUF response with the FSM of sequential circuits," In *Proc. 21st Annual International Symposium on Field-Programmable Custom Computing Machines (FCCM)*, Seattle, USA, 2013, pp. 227.
- [C1] J Zhang, Y Lin, Y Lyu, G Qu, RCC Cheung, **W. Che**, Q Zhou, J Bian "FPGA IP protection by binding finite state machine to physical unclonable function," in *Proc. 23rd Int. Conf. Field Program. Logic Appl. (FPL)*, Porto, Portugal, 2013, pp. 1-4.

### **Poster**

- [P1] **W. Che**, F. Saqib, J. Plusquellic, "A Novel Offset Technique for Improving Bitstring Quality of a Hardware-Embedded Delay PUF," in *IEEE International Symposium on Hardware Oriented Security and Trust (HOST)*, 2017, pp. 157.

### **Patents**

1. "ATPG-Driver Entropy Optimization for a Hardware-Embedded Delay PUF", (STC UNM Ref No. 2016-055).
2. "PUF Authentication Protocols", (STC.UNM Ref No. 2016-056).
3. "Novel Methods designed to improve Entropy and Statistical Quality metrics in PUF generated bitstring", (STC.UNM Ref No. 2017-035)

### **Professional Service**

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### **Conference Session Chair**

- 2019 IEEE/ACM International Conference on Computer-Aided Design (ICCAD)

### **Editorial Board Member**

- MDPI Journal of Cryptography

### **Reviewer**

- IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)
- IEEE Transactions on Information Forensics and Security (TIFS)
- IEEE Transactions on Very Large Scale Integration Systems (TVLSI)
- IEEE Transactions on Dependable and Secure Computing (TDSC)
- IEEE Transactions on Multi-Scale Computing Systems (TMSCS)
- ACM Journal of Emerging Technologies in Computing Systems (ACM JETC)
- ACM Transactions on Embedded Computing Systems (ACM TECS)
- IEEE Internet of Things Journal
- Journal of Hardware and Systems Security
- Sensors

### **Teaching Experience**

- Instructor, EE Selected Topic 490/590 “Hardware Security and Trust”, 18’Fall, 19’Fall  
New Mexico State University, Las Cruces, New Mexico.
- Instructor, EE 112 “Embedded Systems”, 19’Spring, 20’Spring  
New Mexico State University, Las Cruces, New Mexico.

### **Presentations & Demonstrations:**

1. “A non-volatile memory based PUF eliminating helper data”, *33<sup>rd</sup> International Conference on Computer Aided Design (ICCAD)*, San Jose, CA, 2014.
2. “PUF-based Authentication”, *IEEE International Symposium on Hardware Oriented Security and Trust (HOST)*, Washington DC, 2016,
3. “Supply Chain and IoT PUF-based Authentication”, *IEEE International Symposium on Hardware Oriented Security and Trust (HOST)*, Washington DC, 2017. (**Awarded 2<sup>nd</sup> place in hardware demo competition**)

### **Honors and Awards**

- **Awarded 2<sup>nd</sup> Place in Hardware Demo Competition among 26 Groups** in 10<sup>th</sup> IEEE International Symposium on Hardware Oriented Security and Trust (HOST), May 2017.
- **Student Travel Grant** for 9<sup>th</sup> IEEE International Symposium on Hardware Oriented Security and Trust (HOST), May 2016.
- **Student Research Grant (SRG)**, University of New Mexico, 2014
- **Provincial-level Merit Student**, 2009.
- **National Scholarship**, 2007.